

BMW Z4 14" Schematics Document

Ivy/Sandy Bridge Panther Point

2012-04-02

REV : A00

DY : None Installed

UMA: UMA only installed

SG: PX solution installed.

<Core Design>



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Title

Cover Page

Size
A3

Document Number

BMW Z4 DIS

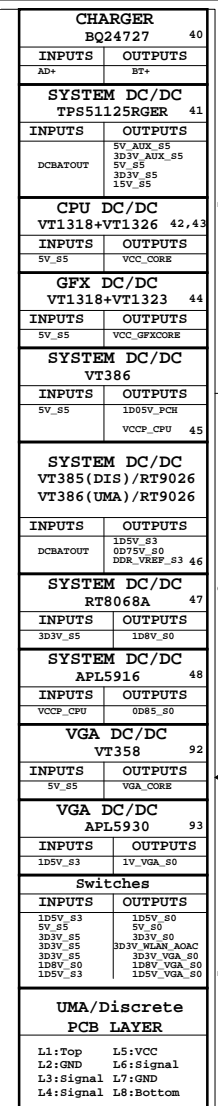
Rev

A00

Date: Monday, April 02, 2012

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Project Code: 91.4UV01.001
PCB P/N : 48.4SB02.011
Revision : 11289-1



PCH Strapping

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature).
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
INTVRMEN	Integrated 1 V VRMs is enabled when high, External when low.
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
DF_TVS	DF_TVS needs to be pulled up to VccDFTerm power rail through 2.2 kOhms ±5% resistor.
HAD_DOCK_EN# /GPIO[33]	This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel HD Audio dock signals to the corresponding Panther Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (0) Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

Power Plane

Power Plane	Voltage	Active Status	Description
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1V_S0 0D85V_S0 0D75V_S0 VCC_CORE VCC GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1V 0.85V 0.75V 0.3V to 1.3V 0 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

Chief River Schematic Checklist Rev.0_72

Sandy & Ivy Bridge Compatibility

Pin Name	Configuration	Schematic Notes
DDR3 VREF	Sandy Bridge + Ivy Bridge	DDR3 VREF, M1 and M3 function are required.
	Ivy Bridge	No change.
PROC_SELECT# & DF_TVS	Sandy Bridge + Ivy Bridge	Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 1K±5% series resistor. PROC_SELECT# also needs a 2.2K±5% pull up resistor to PCH VccDFTerm rail.
	Ivy Bridge	No change.
VCCIO_SEL	Sandy Bridge + Ivy Bridge	The POR for Ivy Bridge mobile parts is now 1.05 V. There is no longer a need for a separate VR for the processor at 1.0 V and the PCH at 1.05 V. A single VR may be shared for both.
	Ivy Bridge	No change.
VCCSA_VID[0:1]	Sandy Bridge + Ivy Bridge	VCCSA[0:1] are the select pin of VCCSA's power control.
	Ivy Bridge	No change.

Chief River Schematic Checklist Rev.0_xx

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value	POP Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1	0
CFG[4]		1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connectd to the EMBEDDED display Port	1	1
CFG[6:5]	PCI-Express Port Bifurcation Straps	11: 1x16 PCI Express 10: 2 x8 - PCI Express 01: Reserved 00: 1x8, 2x4 PCI Express	11	10

Chief River Schematic Checklist Rev.0_72

USB Table

Pair	Device
0	USB3.0 port1, with Power Share
1	USB3.0 port2, debug port
2	NC
3	NC
4	Touch Panel
5	NC
6	NC
7	NC
8	WWAN
9	NC
10	Card reader
11	WLAN
12	CAMERA
13	NC

PCIE Table

PCIE	
Lane	Device
1	NC
2	NC
3	NC
4	WLAN
5	NC
6	Onboard LAN
7	NC
8	NC

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	NC
3	NC
4	ODD
5	NC

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Layout Note:

DMI trace length 2000~8000mil

Layout Note:

FDI trace length 2000~6500mil

Layout Note:

Signal Routing Guideline:

EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

Layout Note:

PEG trace length 1500~9000mil

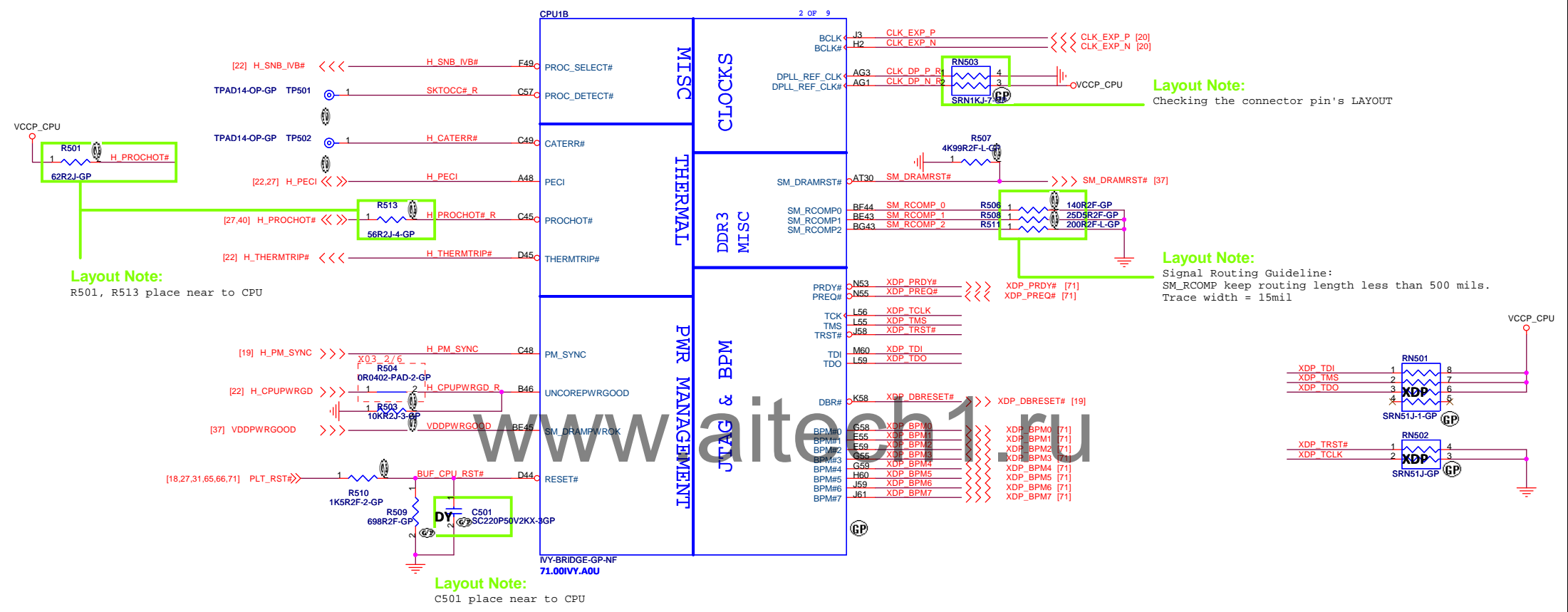
- **Layout Note:**

Signal Routing Guideline:

PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.

PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

SSID = CPU



SSID = CPU

[14] M_A_DQ[63:0] <<>> M_A_DQ[63:0]

CPU1C

3 OF 9

M_A_DQ0 AG6 SA_DQ0
M_A_DQ1 AJ6 SA_DQ1
M_A_DQ2 AL6 SA_DQ2
M_A_DQ3 AL6 SA_DQ3
M_A_DQ4 AJ10 SA_DQ4
M_A_DQ5 AJ8 SA_DQ5
M_A_DQ6 AL8 SA_DQ6
M_A_DQ7 AL7 SA_DQ7
M_A_DQ8 AR11 SA_DQ8
M_A_DQ9 AP6 SA_DQ9
M_A_DQ10 AU6 SA_DQ10
M_A_DQ11 AV9 SA_DQ11
M_A_DQ12 AR6 SA_DQ12
M_A_DQ13 AP8 SA_DQ13
M_A_DQ14 AT13 SA_DQ14
M_A_DQ15 AU13 SA_DQ15
M_A_DQ16 BC7 SA_DQ16
M_A_DQ17 BB7 SA_DQ17
M_A_DQ18 BA13 SA_DQ18
M_A_DQ19 BB11 SA_DQ19
M_A_DQ20 BA7 SA_DQ20
M_A_DQ21 BA9 SA_DQ21
M_A_DQ22 BB9 SA_DQ22
M_A_DQ23 AY13 SA_DQ23
M_A_DQ24 AV14 SA_DQ24
M_A_DQ25 AR14 SA_DQ25
M_A_DQ26 AY17 SA_DQ26
M_A_DQ27 AR19 SA_DQ27
M_A_DQ28 BA14 SA_DQ28
M_A_DQ29 AU14 SA_DQ29
M_A_DQ30 BB14 SA_DQ30
M_A_DQ31 BB17 SA_DQ31
M_A_DQ32 BA45 SA_DQ32
M_A_DQ33 AR43 SA_DQ33
M_A_DQ34 AU48 SA_DQ34
M_A_DQ35 BC48 SA_DQ35
M_A_DQ36 BC45 SA_DQ36
M_A_DQ37 AR45 SA_DQ37
M_A_DQ38 AT48 SA_DQ38
M_A_DQ39 AY48 SA_DQ39
M_A_DQ40 BA49 SA_DQ40
M_A_DQ41 AV49 SA_DQ41
M_A_DQ42 BB51 SA_DQ42
M_A_DQ43 AY53 SA_DQ43
M_A_DQ44 BB49 SA_DQ44
M_A_DQ45 AU49 SA_DQ45
M_A_DQ46 BA53 SA_DQ46
M_A_DQ47 BB55 SA_DQ47
M_A_DQ48 BA55 SA_DQ48
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M_A_DQ51 AP53 SA_DQ51
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M_A_DQ53 AT54 SA_DQ53
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M_A_DQ55 AP52 SA_DQ55
M_A_DQ56 AN57 SA_DQ56
M_A_DQ57 AN53 SA_DQ57
M_A_DQ58 AG56 SA_DQ58
M_A_DQ59 AG53 SA_DQ59
M_A_DQ60 AN52 SA_DQ60
M_A_DQ61 AG55 SA_DQ61
M_A_DQ62 AK56 SA_DQ62
M_A_DQ63 AK56 SA_DQ63

DDR SYSTEM MEMORY A

SA_CK0 AU36
SA_CK#0 AY26
SA_CKE0 AY26

SA_CK1 AT40
SA_CK#1 AU40
SA_CKE1 BB26

SA_CS#0 BB40
SA_CS#1 BC41

SA_ODT0 AY40
SA_ODT1 BA41

SA_DQS#0 AL11
SA_DQS#1 AR8
SA_DQS#2 AV11
SA_DQS#3 AT17
SA_DQS#4 AV45
SA_DQS#5 AY51
SA_DQS#6 AT55
SA_DQS#7 AK55

SA_DQS0 AL11
SA_DQS1 AR10
SA_DQS2 AY11
SA_DQS3 AU17
SA_DQS4 AW45
SA_DQS5 AV51
SA_DQS6 AT56
SA_DQS7 AK54

SA_MA0 BG35
SA_MA1 BB34
SA_MA2 BE35
SA_MA3 BD35
SA_MA4 AT34
SA_MA5 AU34
SA_MA6 BB32
SA_MA7 AT32
SA_MA8 AY32
SA_MA9 AV32
SA_MA10 BE37
SA_MA11 BA30
SA_MA12 BC30
SA_MA13 AW41
SA_MA14 AY28
SA_MA15 AU26

M_A_DIMA_CLK_DDR0 [14]
M_A_DIMA_CLK_DDR#0 [14]
M_A_DIMA_CKE0 [14]

M_A_DIMA_CLK_DDR1 [14]
M_A_DIMA_CLK_DDR#1 [14]
M_A_DIMA_CKE1 [14]

M_A_DIMA_CS#0 [14]
M_A_DIMA_CS#1 [14]

M_A_DIMA_ODT0 [14]
M_A_DIMA_ODT1 [14]

M_A_DQS#0 [14]
M_A_DQS#1 [14]
M_A_DQS#2 [14]
M_A_DQS#3 [14]
M_A_DQS#4 [14]
M_A_DQS#5 [14]
M_A_DQS#6 [14]
M_A_DQS#7 [14]

M_A_DQS#0 [14]
M_A_DQS#1 [14]
M_A_DQS#2 [14]
M_A_DQS#3 [14]
M_A_DQS#4 [14]
M_A_DQS#5 [14]
M_A_DQS#6 [14]
M_A_DQS#7 [14]

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M_A_A1 [14]
M_A_A2 [14]
M_A_A3 [14]
M_A_A4 [14]
M_A_A5 [14]
M_A_A6 [14]
M_A_A7 [14]
M_A_A8 [14]
M_A_A9 [14]
M_A_A10 [14]
M_A_A11 [14]
M_A_A12 [14]
M_A_A13 [14]
M_A_A14 [14]
M_A_A15 [14]



IVY-BRIDGE-GP-NF
71.00IVY.A0U

[15] M_B_DQ[63:0] <<>> M_B_DQ[63:0]

CPU1D

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M_B_DQ0 AL4 SB_DQ0
M_B_DQ1 AL1 SB_DQ1
M_B_DQ2 AN3 SB_DQ2
M_B_DQ3 AR3 SB_DQ3
M_B_DQ4 AK4 SB_DQ4
M_B_DQ5 AK3 SB_DQ5
M_B_DQ6 AN4 SB_DQ6
M_B_DQ7 AR1 SB_DQ7
M_B_DQ8 AU4 SB_DQ8
M_B_DQ9 AT2 SB_DQ9
M_B_DQ10 AV4 SB_DQ10
M_B_DQ11 BA4 SB_DQ11
M_B_DQ12 AU3 SB_DQ12
M_B_DQ13 AR3 SB_DQ13
M_B_DQ14 AY2 SB_DQ14
M_B_DQ15 BA3 SB_DQ15
M_B_DQ16 BE9 SB_DQ16
M_B_DQ17 BD9 SB_DQ17
M_B_DQ18 BD13 SB_DQ18
M_B_DQ19 BF12 SB_DQ19
M_B_DQ20 BF8 SB_DQ20
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M_B_DQ22 BE13 SB_DQ22
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M_B_DQ30 BG18 SB_DQ30
M_B_DQ31 BF19 SB_DQ31
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M_B_DQ33 BF48 SB_DQ33
M_B_DQ34 BD53 SB_DQ34
M_B_DQ35 BE52 SB_DQ35
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M_B_DQ41 BE57 SB_DQ41
M_B_DQ42 BC59 SB_DQ42
M_B_DQ43 AY60 SB_DQ43
M_B_DQ44 BE54 SB_DQ44
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M_B_DQ48 AU59 SB_DQ48
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M_B_DQ60 AM60 SB_DQ60
M_B_DQ61 AL59 SB_DQ61
M_B_DQ62 AF61 SB_DQ62
M_B_DQ63 AH60 SB_DQ63

DDR SYSTEM MEMORY B

SB_CK0 BA34
SB_CK#0 AY34
SB_CKE0 AR22

SB_CK1 BA36
SB_CK#1 BB36
SB_CKE1 BF27

SB_CS#0 BE41
SB_CS#1 BE47

SB_ODT0 AT43
SB_ODT1 BG47

SB_DQS#0 AL3
SB_DQS#1 AV3
SB_DQS#2 BG11
SB_DQS#3 BD17
SB_DQS#4 BG51
SB_DQS#5 BA59
SB_DQS#6 AT60
SB_DQS#7 AK59

SB_DQS0 AM2
SB_DQS1 AV1
SB_DQS2 BE11
SB_DQS3 BD18
SB_DQS4 BE51
SB_DQS5 BA61
SB_DQS6 AR59
SB_DQS7 AK61

SB_MA0 BF32
SB_MA1 BE33
SB_MA2 BD33
SB_MA3 AU30
SB_MA4 BD30
SB_MA5 AV30
SB_MA6 BG30
SB_MA7 RD29
SB_MA8 BE30
SB_MA9 BE28
SB_MA10 BD43
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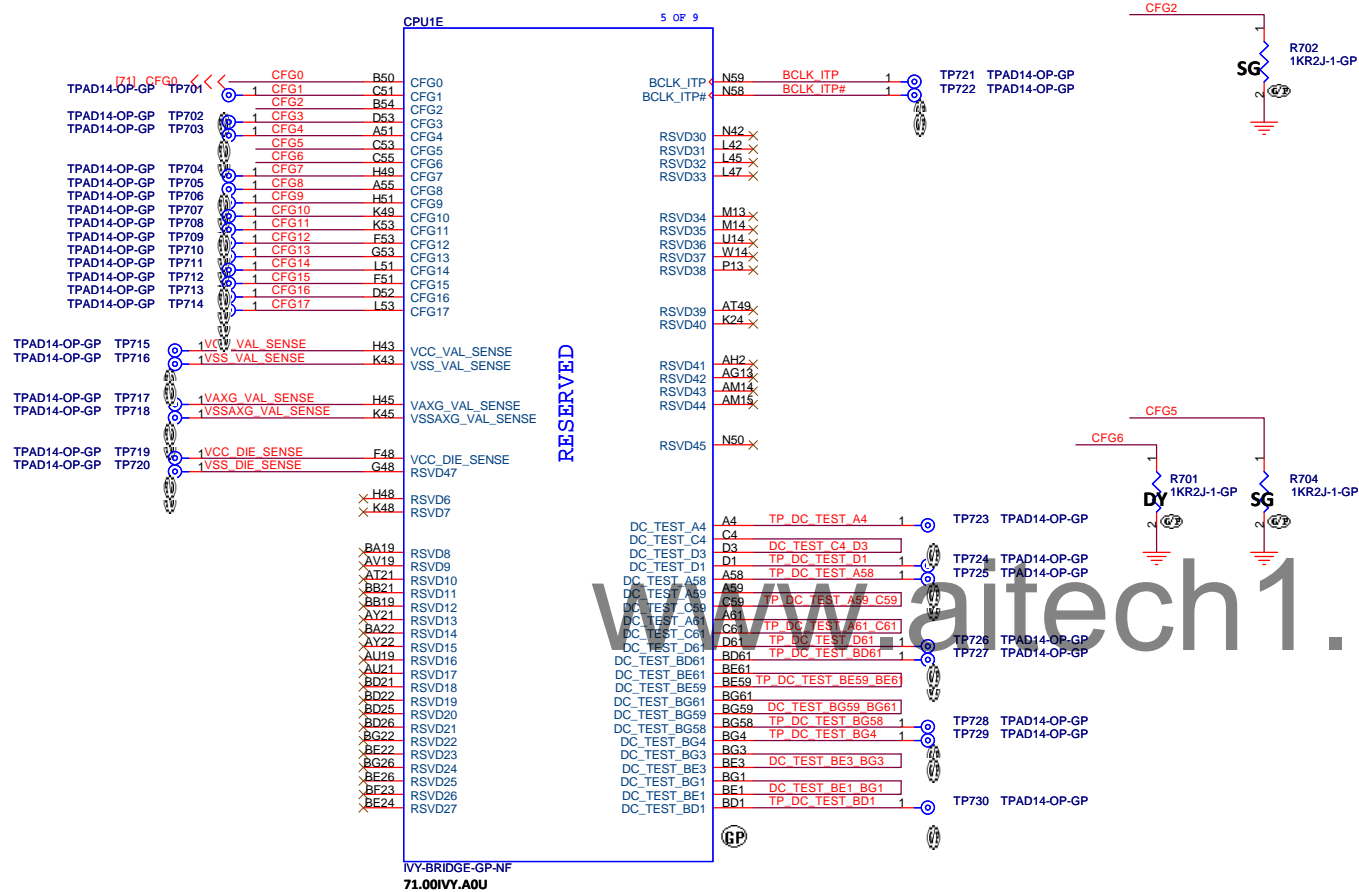
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Title		
CPU (DDR)		
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SSID = CPU



PEG Static Lane Reversal	
CFG[2]	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed

Display Port Presence Strap	
CFG[4]	1: Disabled: No Physical Display Port attached to Embedded Display Port
	0: Enabled: An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	11: 1x16 PCI Express 10: 2 x8 - PCI Express 01: Reserved 00: 1x8, 2x4 PCI Express



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CPU (RESERVED)

Size
A3

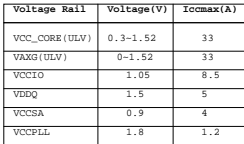
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BMW Z4 DIS

Date: Friday, March 30, 2012

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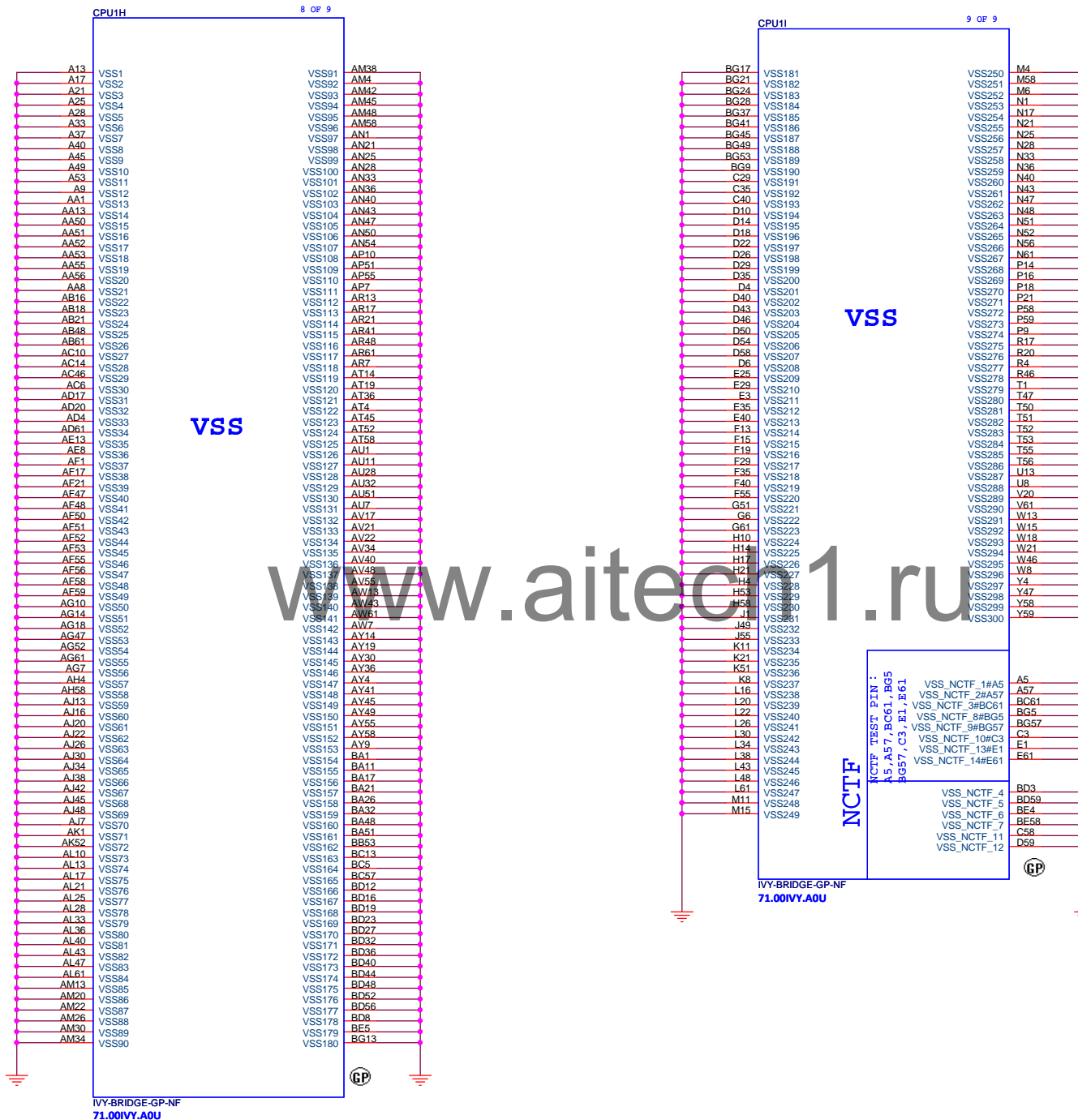
A00 3/30
X01 12/21
X01 12/16
X01 12/15
X01 12/09



- Layout Note:
 1. PH/PL resistors place close CPU
 2. SENSE signal recommend differential routing

- Layout Note:
 1. PH/PL resistors place close CPU
 2. SENSE signal recommend differential routing

SSID = CPU



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Title

CPU (VSS)Size
A3

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XDP

Size
A3

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Title
(Reserved)

Size
A3

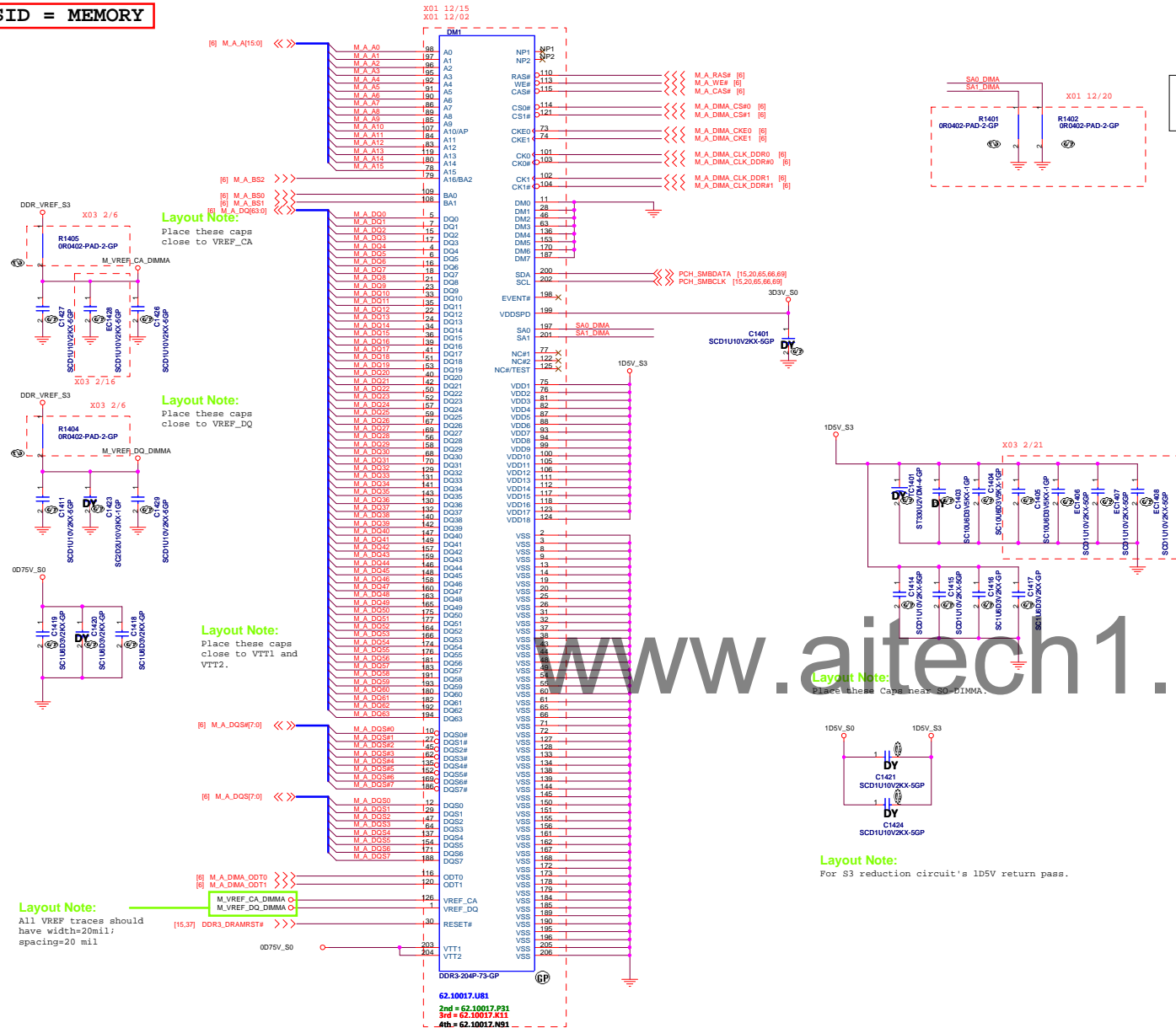
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SSID = MEMORY

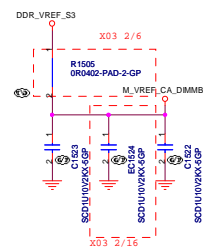


Note:
SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

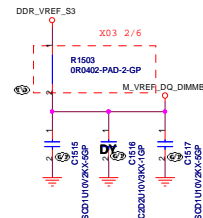
Layout Note:
Place these Caps near SO-DIMM1.

Layout Note:
For S3 reduction circuit's 1D5V return pass.

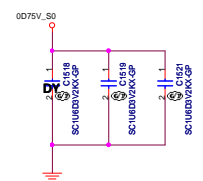
SSID = MEMORY



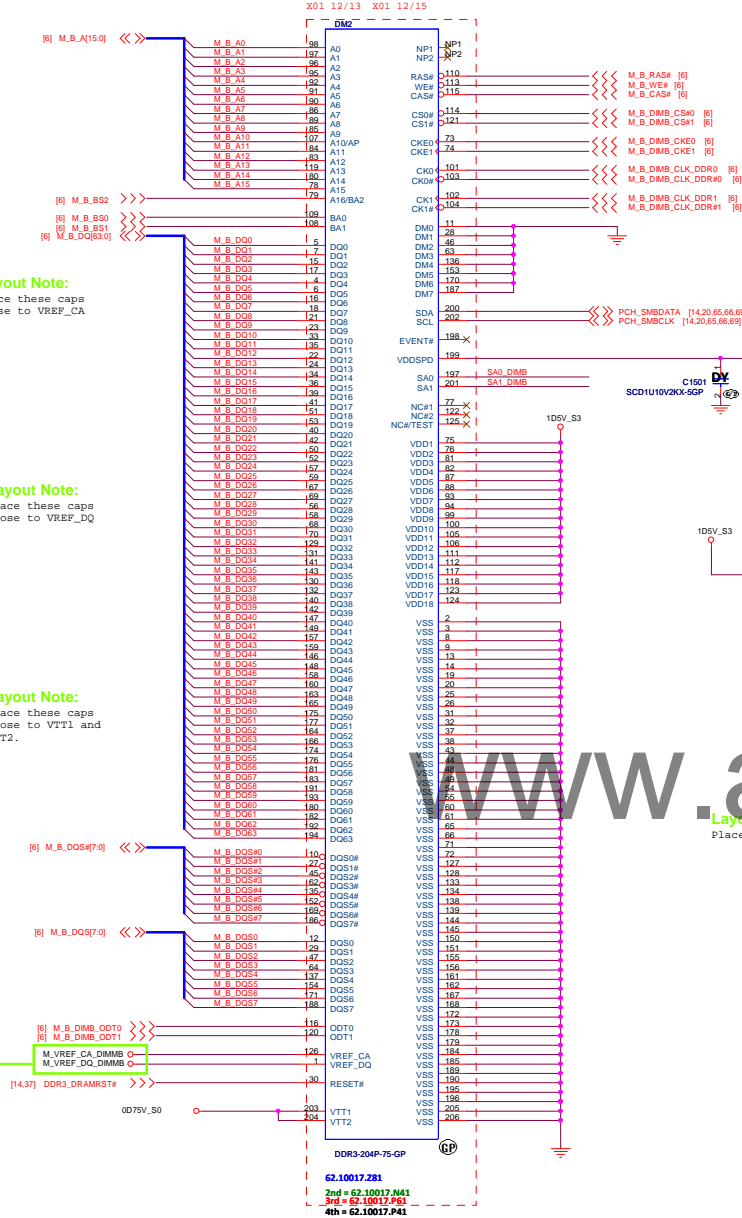
Layout Note:
Place these caps close to VREF.



Layout Note
Place these close to VRE

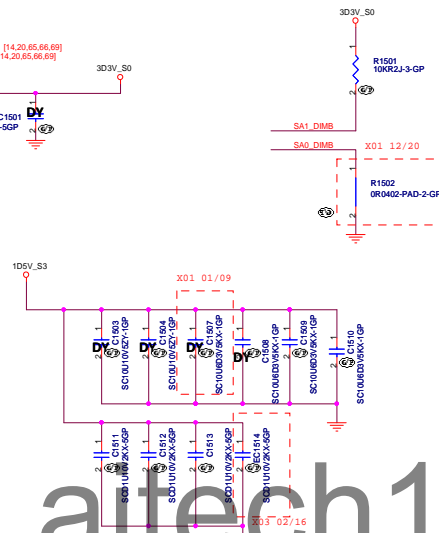


Layout Note:
Place these caps
close to VTT1 and
VTT2.



Layout Note:
Place these Caps near SO-DIMM.

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34



Layout Note:
Place these Caps near SO-DIMM.



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Document Number
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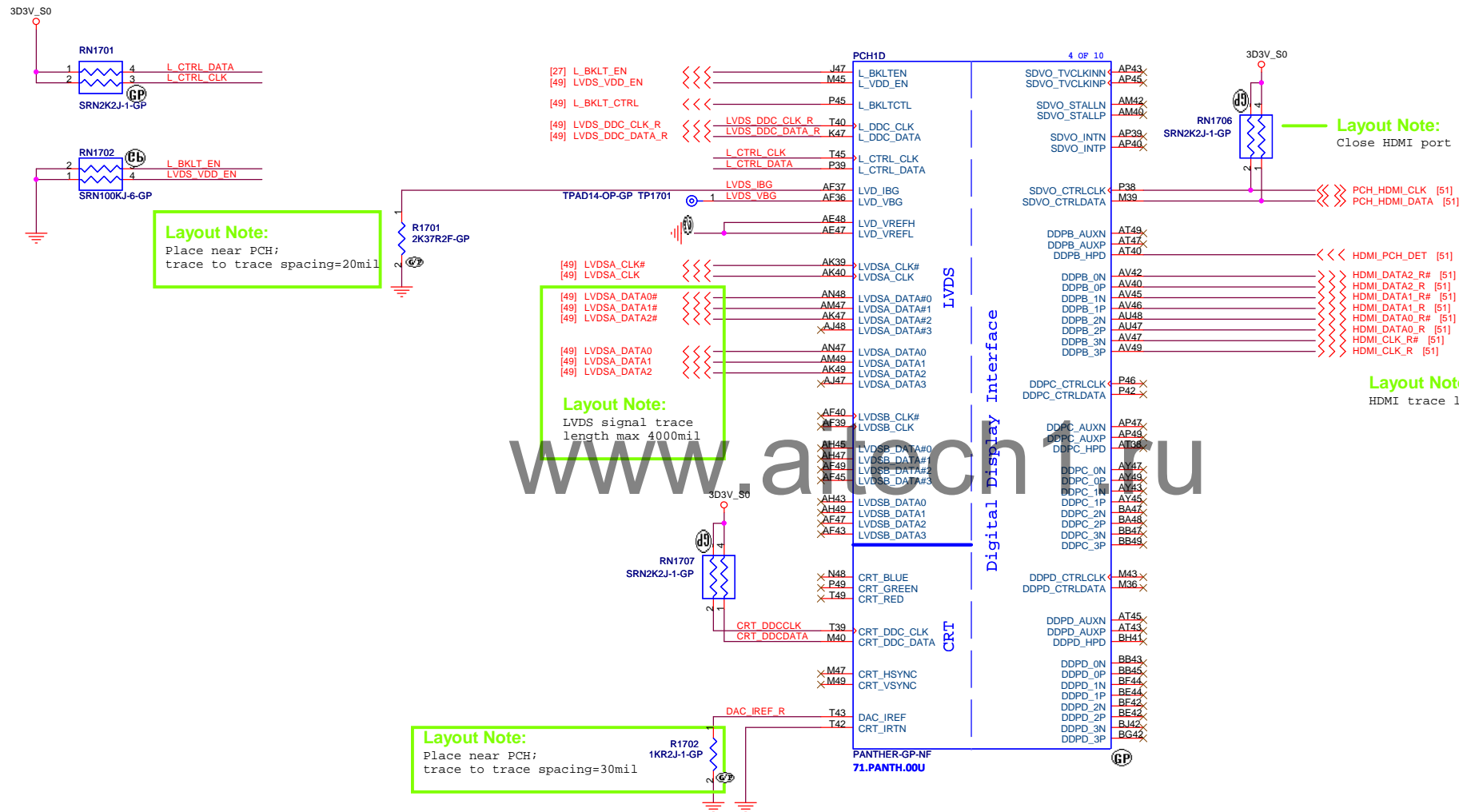
Rev
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Reserved

SSID = PCH



<Core Design>

DELL Wistron Corporation
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Title PCH (LVDS/CRT/DDI)		
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SSID = PCH

USB3.0/2.0 Mapping Table

USB 3.0 Port	USB 2.0 port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

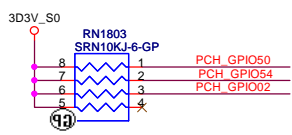
USB Table

Pair	Device
0	USB3.0 port1, with Power Share
1	USB3.0 port2
2	NC
3	NC
4	Touch Panel
5	NC
6	NC
7	NC
8	WWAN
9	NC
10	Card reader
11	WLAN
12	CAMERA
13	NC

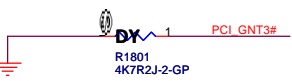
1. USB Ext. port 9 (HS) External debug port use on Chief River platform.
2. 2011 July; Microsoft will support USB3.0 debug--> Port1 useable.

Layout Note:

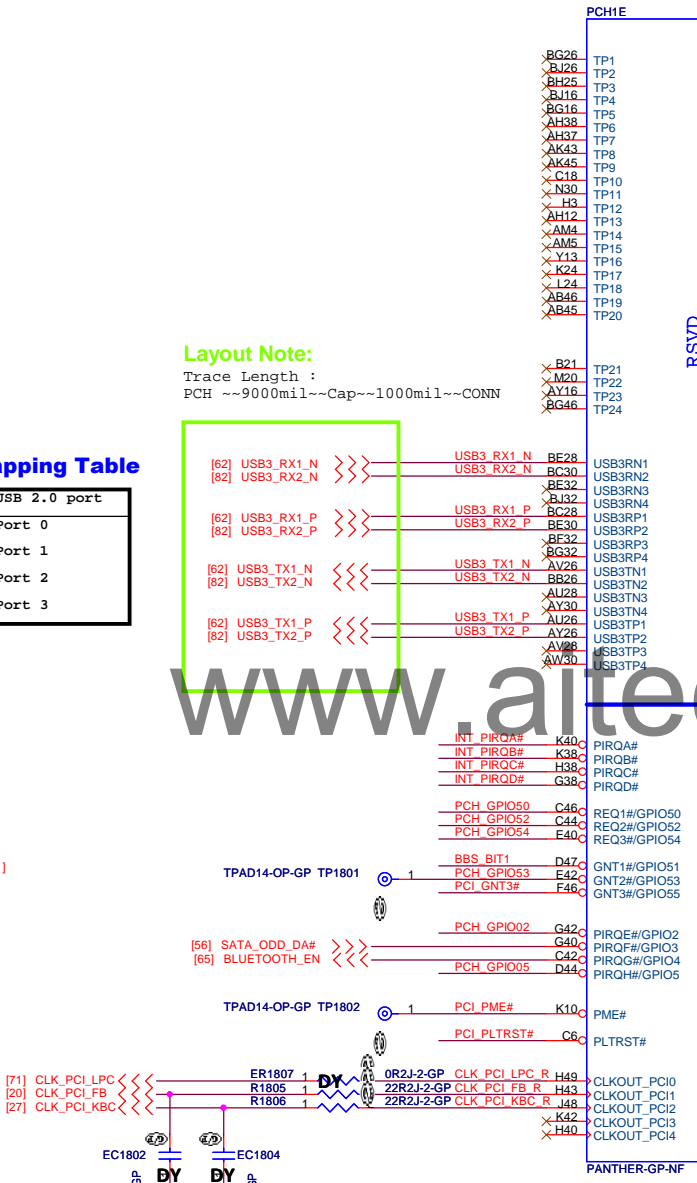
1. USBRBIAS/# use 50ohm single-ended impedance spacing to other signal=15mil
2. Length < 500mil



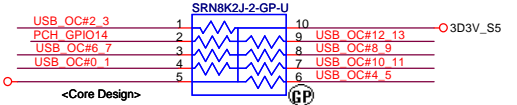
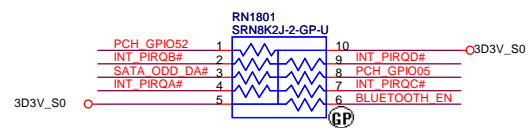
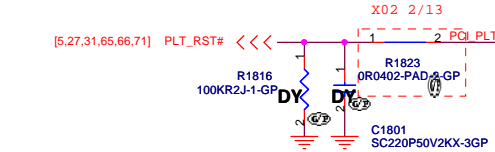
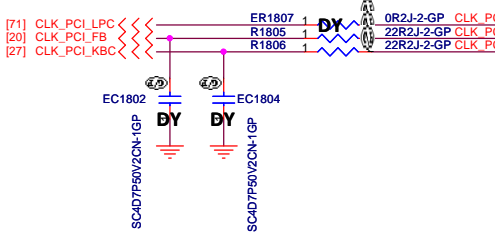
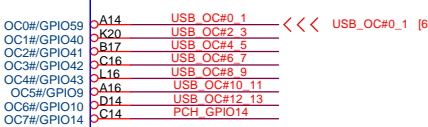
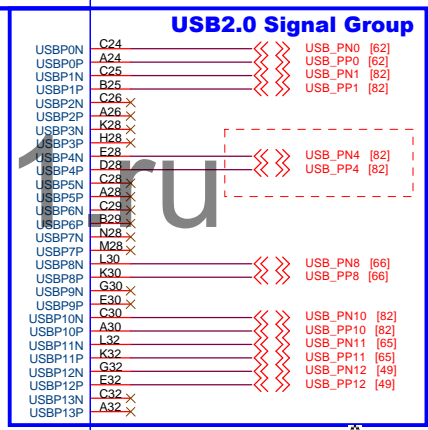
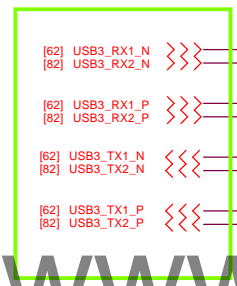
Boot Bios Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



A16 Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



Layout Note:
Trace Length :
PCH ~9000mil~~Cap~~1000mil~~CONN



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File: **PCH (PCI/USB/NVRAM)**

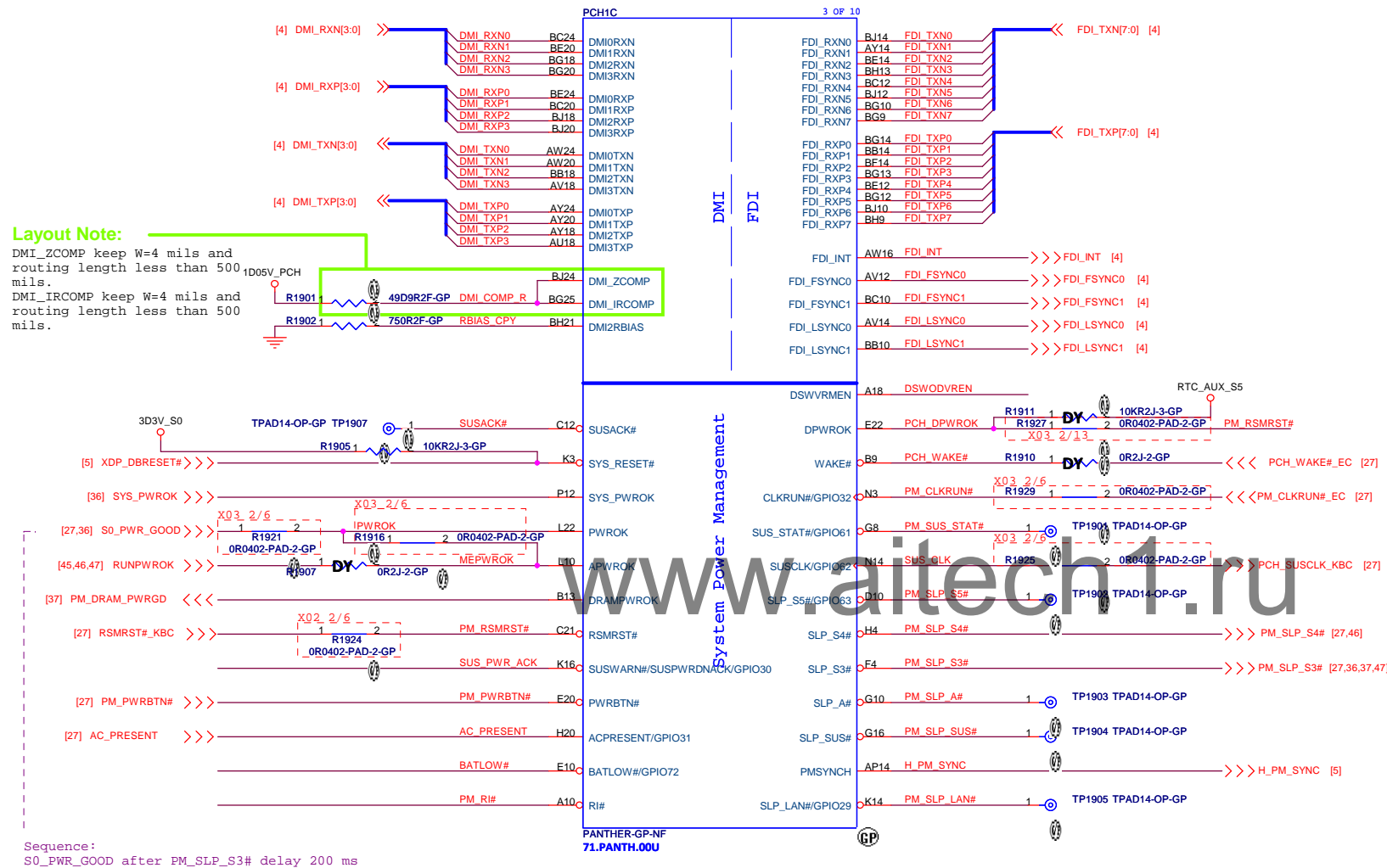
Size A3 Document Number: **BMW Z4 DIS** Rev: **A00**

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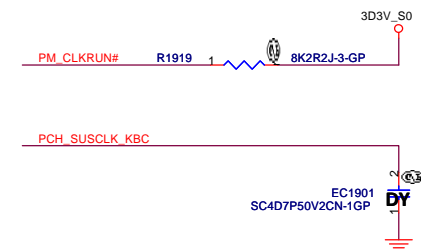
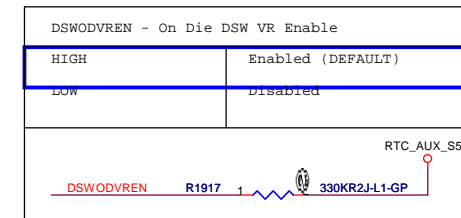
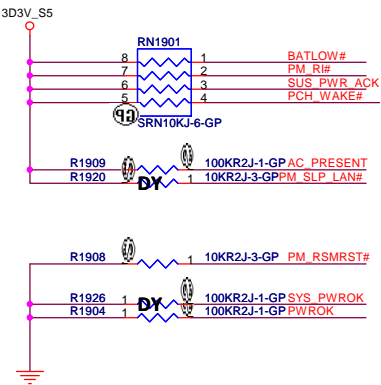
SSID = PCH

Layout Note:

DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



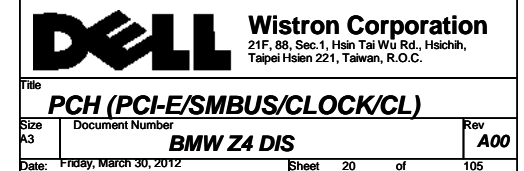
Sequence:
S0_PWR_GOOD after PM_SLP_S3# delay 200 ms



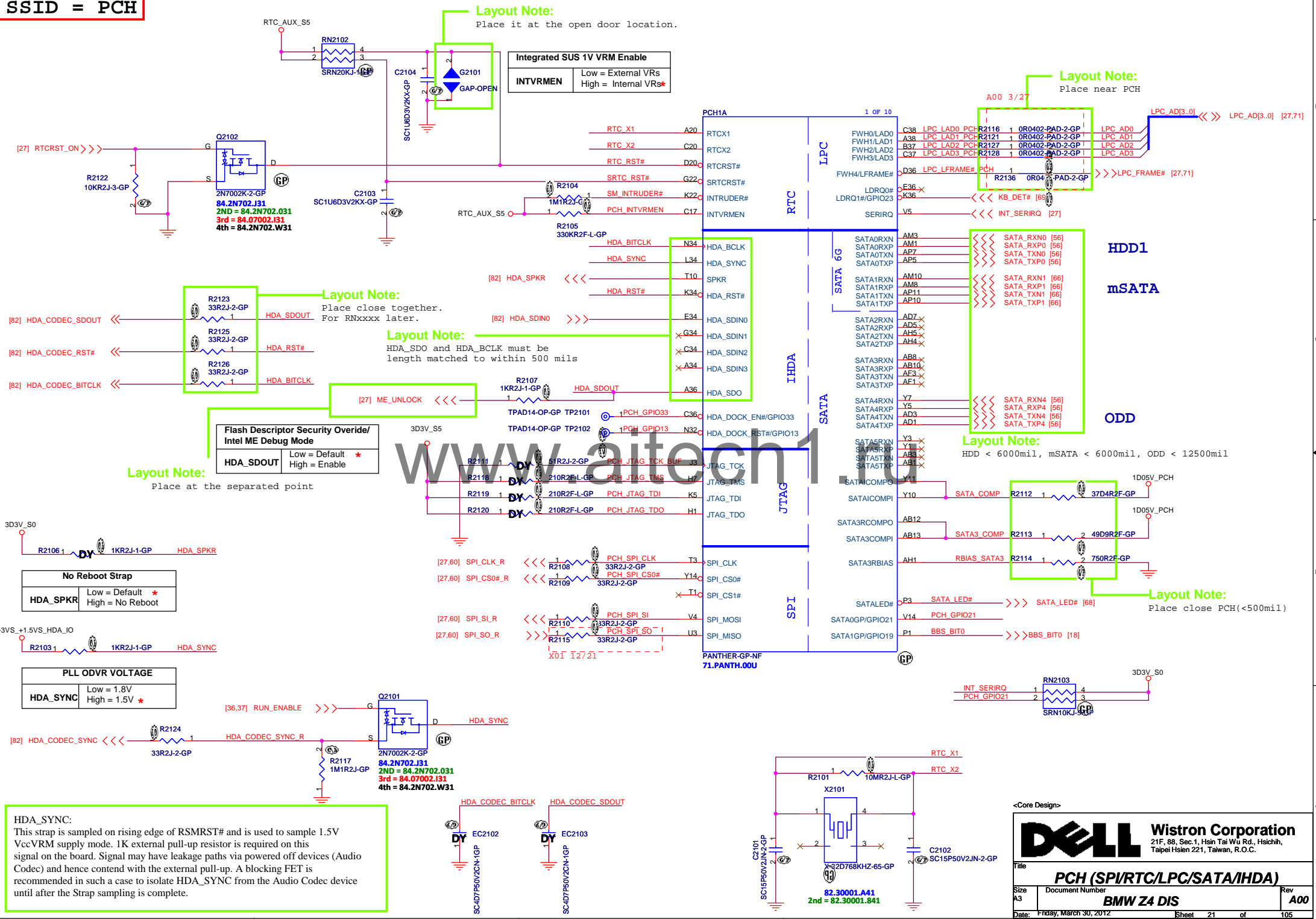
<Core Design>

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Title: PCH (DM I/FDI/PM)			
Size: A3	Document Number: BMW Z4 DIS	Rev: A00	
Date: Friday, March 30, 2012	Sheet: 19	of 105	

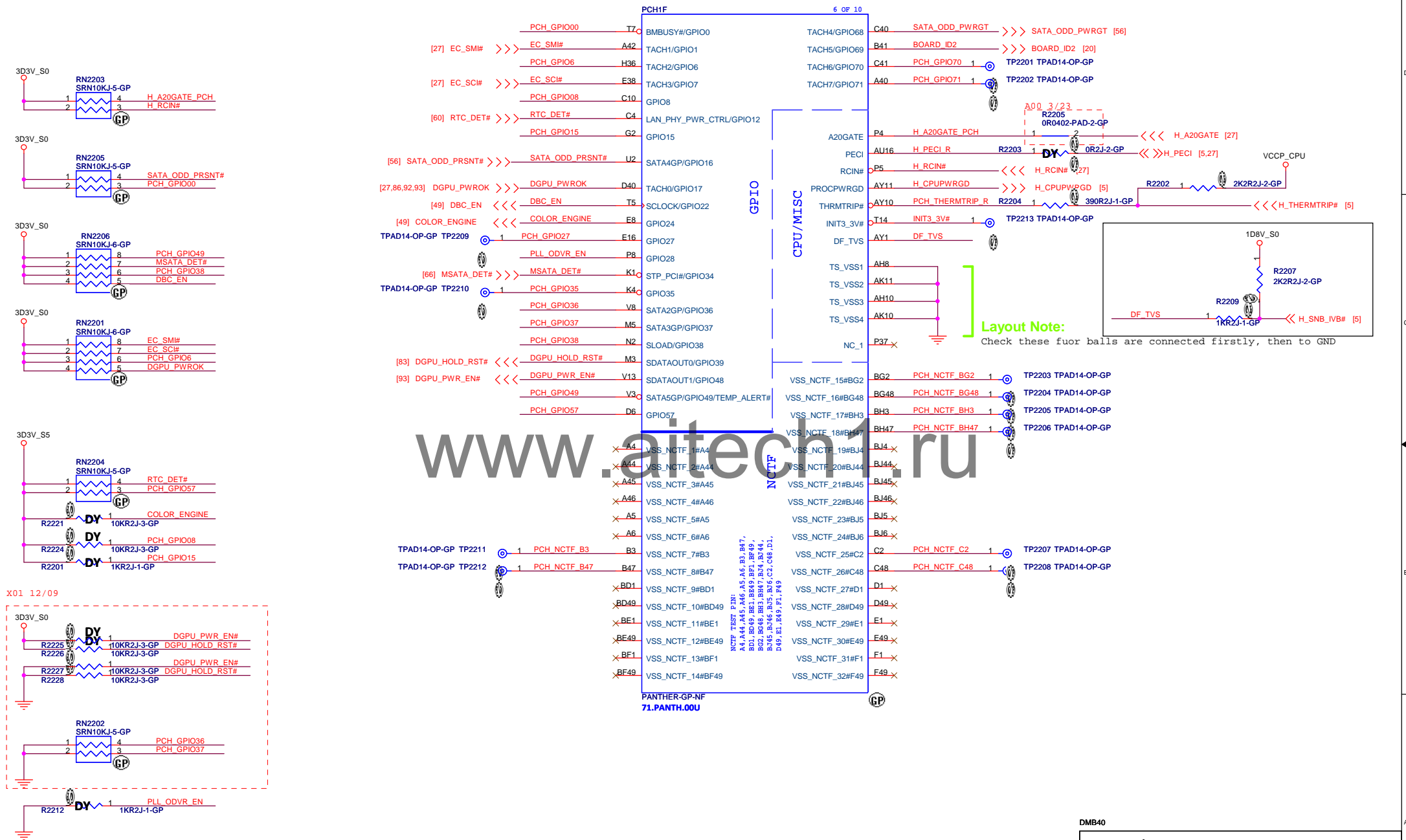
S5 power rail CLKREQ#:
PCIECLKRQ[0]#
PCIECLKRQ[7:3]#



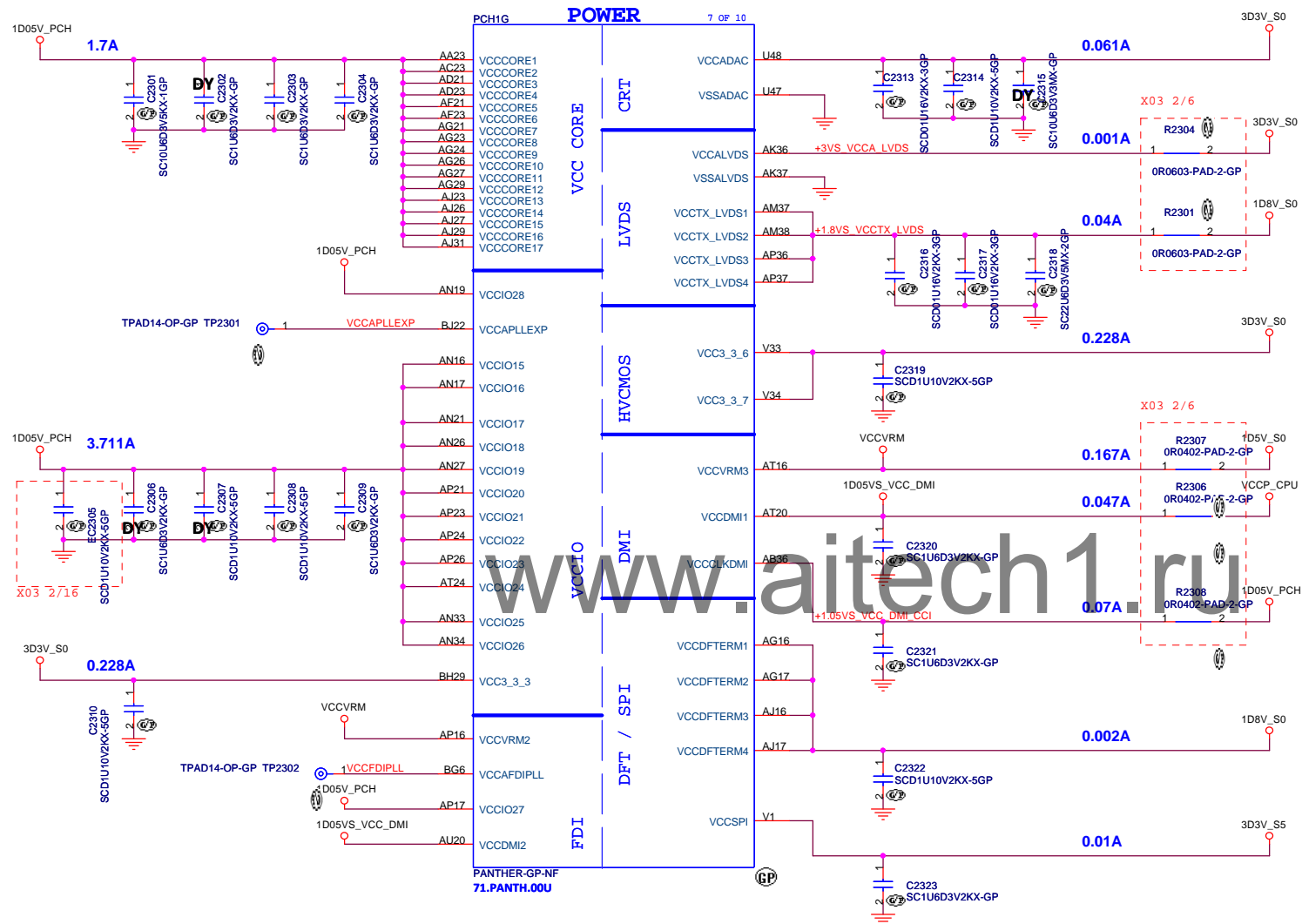
SSID = PCH



SSID = PCH



SSID = PCH



Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKLN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to chipset EDS V.0.7



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Title

PCH (POWER1)

Size

Document Number

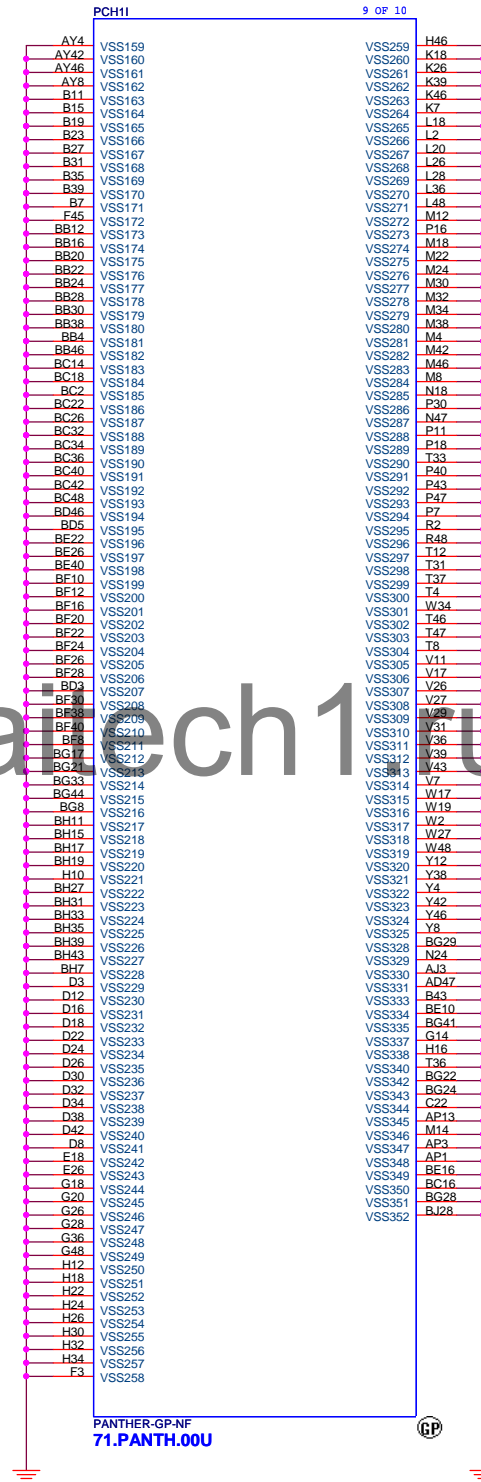
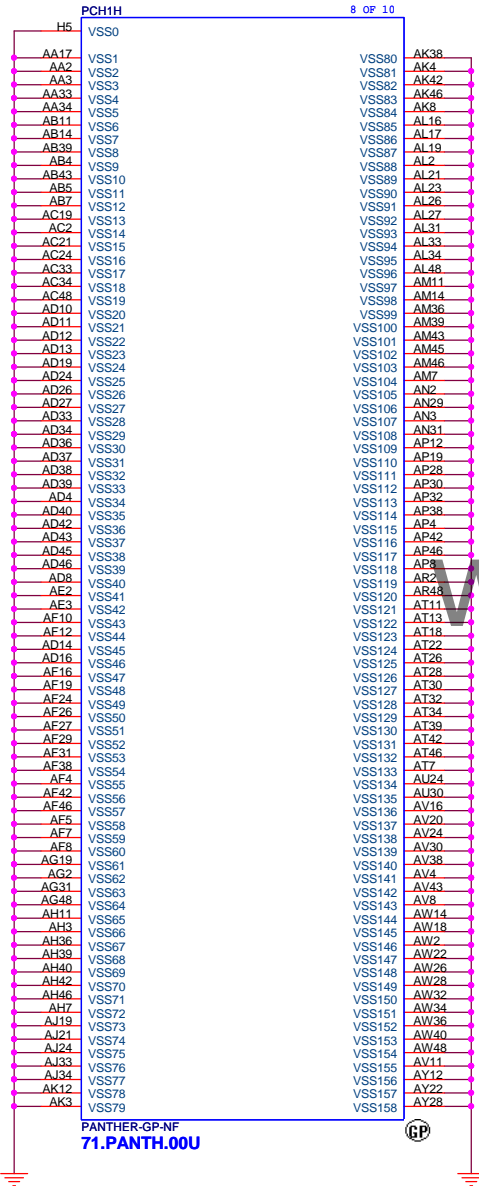
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SSID = PCH



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Title **PCH (VSS)**

Size A3 Document Number **BMW Z4 DIS** Rev **A00**

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Title

Reserved

Size
A3

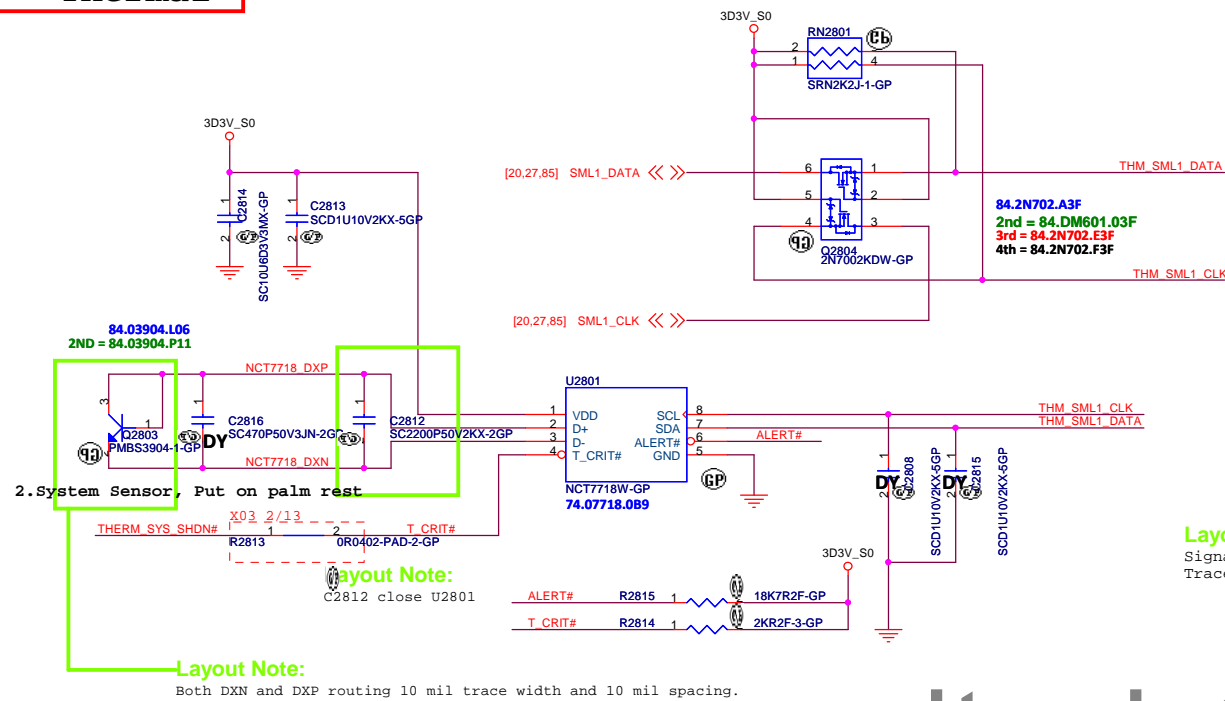
Document Number
BMW Z4 DIS

Date: Friday, March 30, 2012

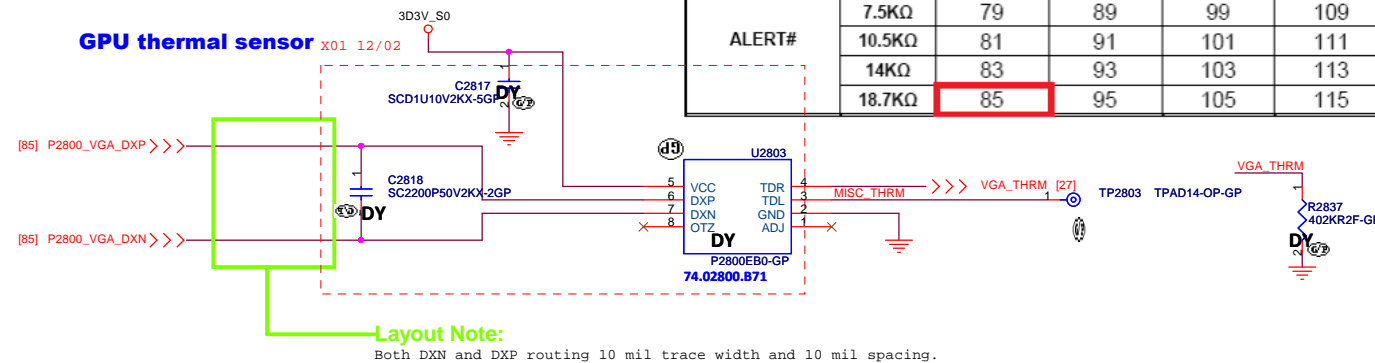
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SSID = Thermal

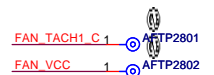


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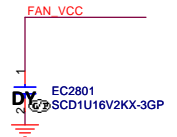


Thermal Sensor	
ADJ	Temp. (C)
Pull high	95
Pull low	90
Floating	85

TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



EMI



<Core Design>

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Title: **Thermal NCT7718W/Fan Controller P2793**


Size A3 Document Number **BMW Z4 DIS** Rev **A00**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
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Document Number
BMW Z4 DIS

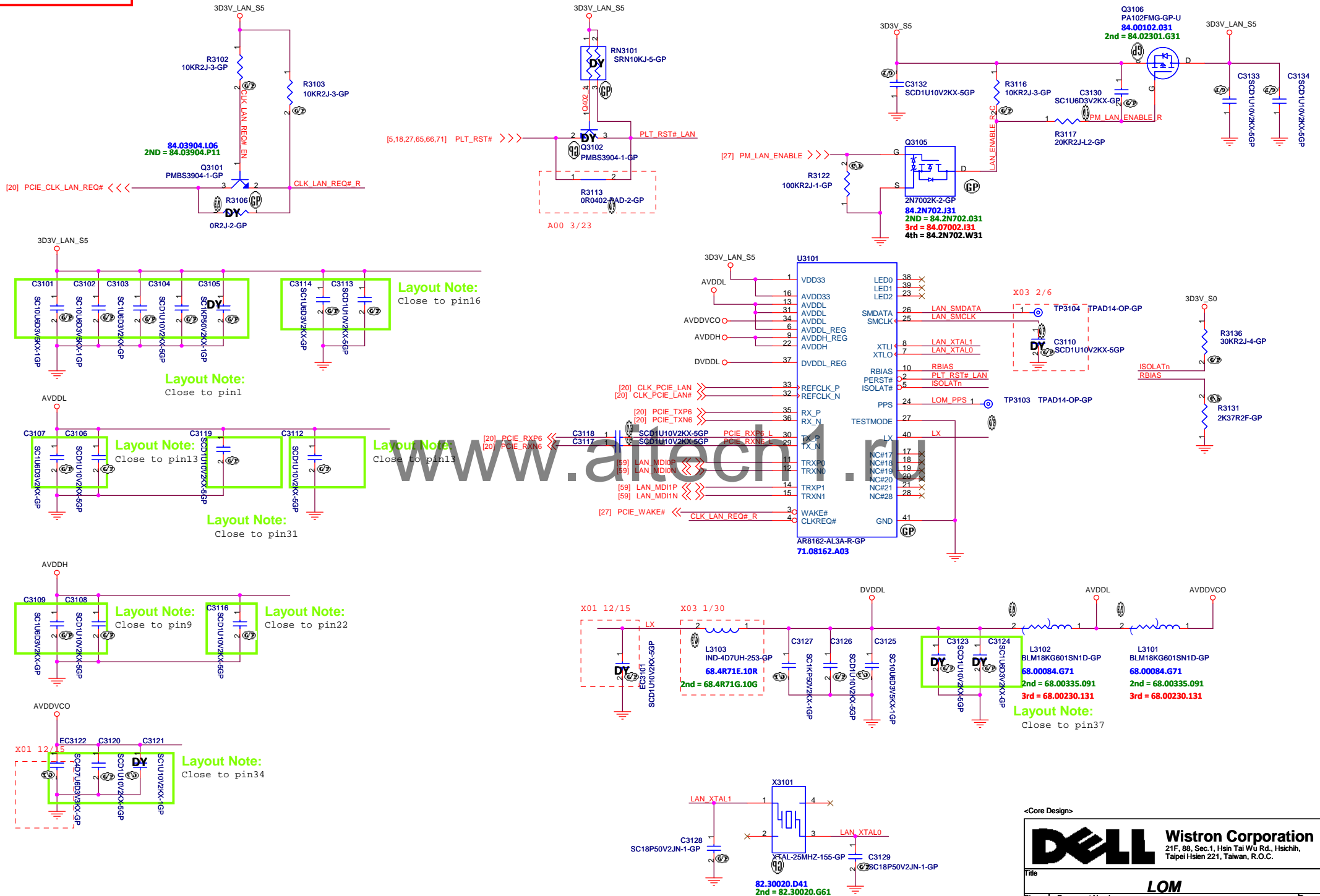
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SSID = LOM



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Title			
Reserved			
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Title

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Title

Reserved

Size
A3

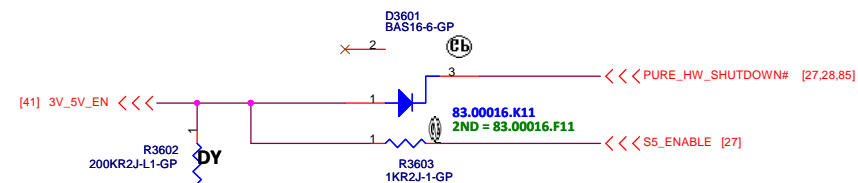
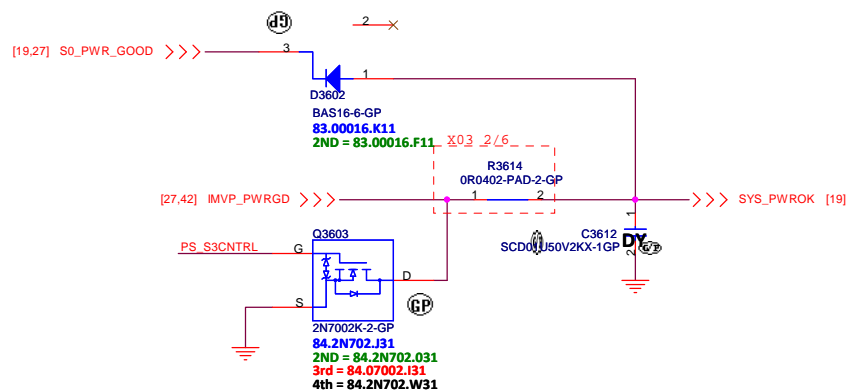
Document Number
BMW Z4 DIS

Rev
A00

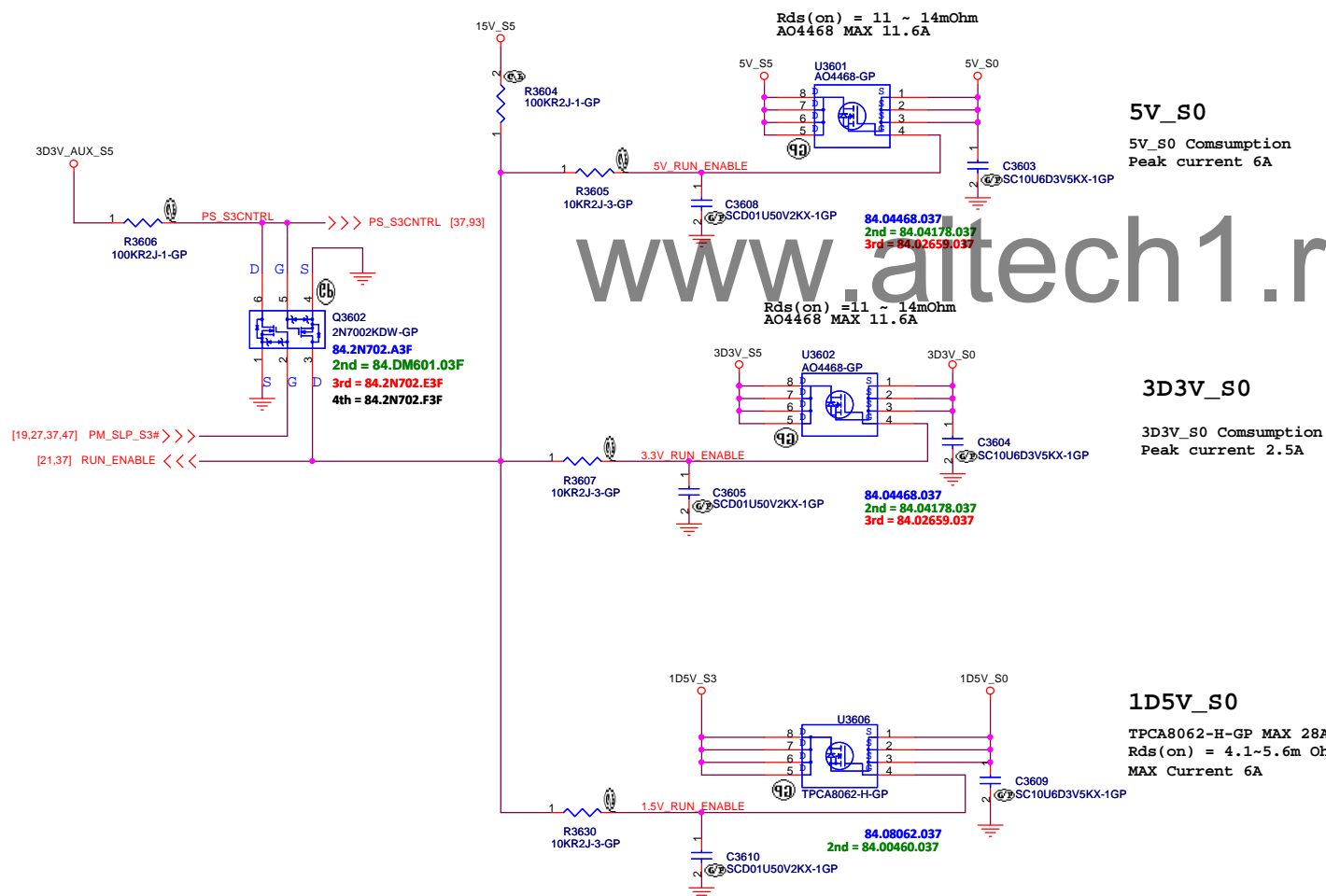
Date: Friday, March 30, 2012

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```
SSID = Reset.Suspend
```



ROSA Run Power



5V S0

5V_S0 Comsumption
Peak current 6A

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

1D5V_S0

TPCA8062-H-GP MAX 28A
Rds(on) = 4.1~5.6m Ohm
MAX Current 6A

<Core Design>



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Title

Power Plane Enable

Size

Document Number

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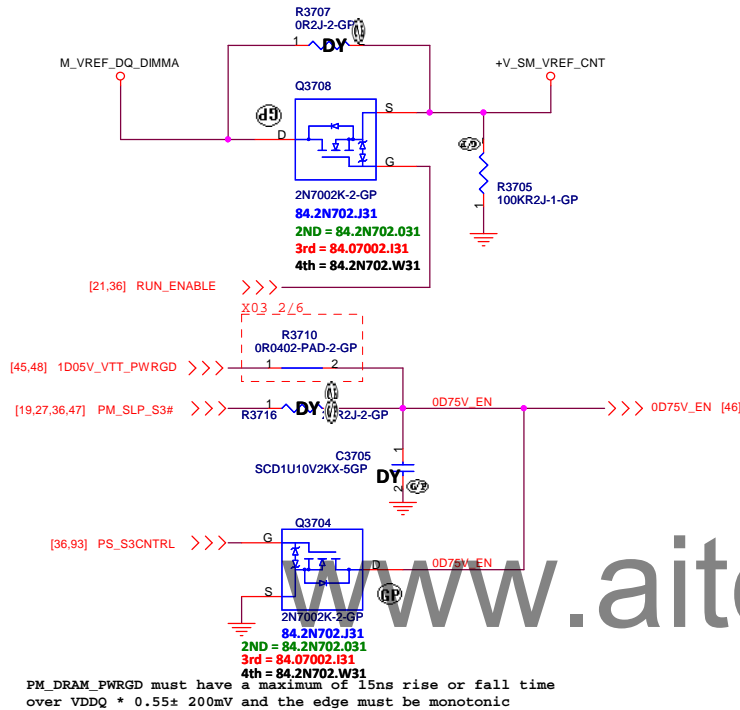
Date: Friday, March 30, 2012

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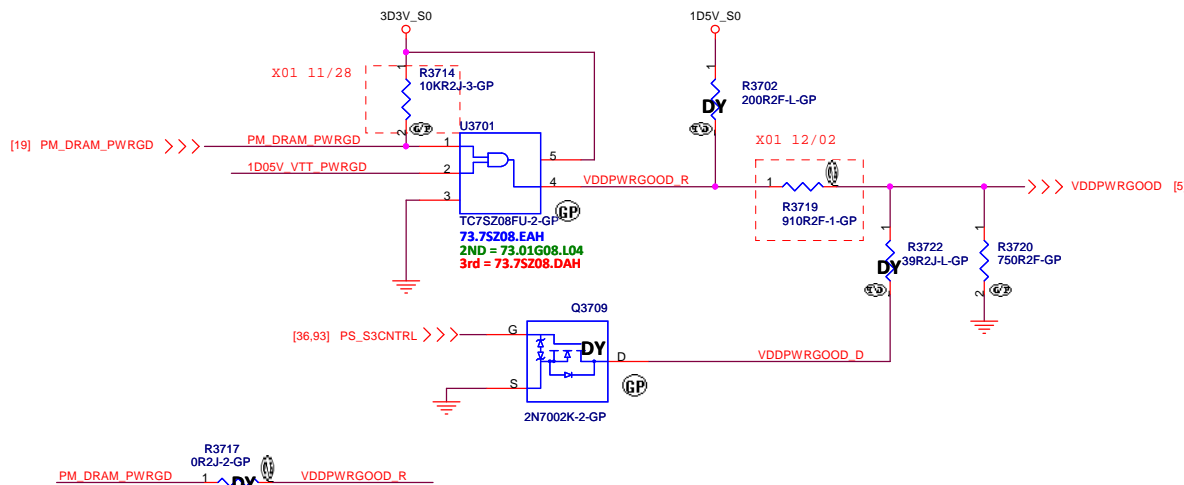
Rev
A00

SSID = Reset.Suspend

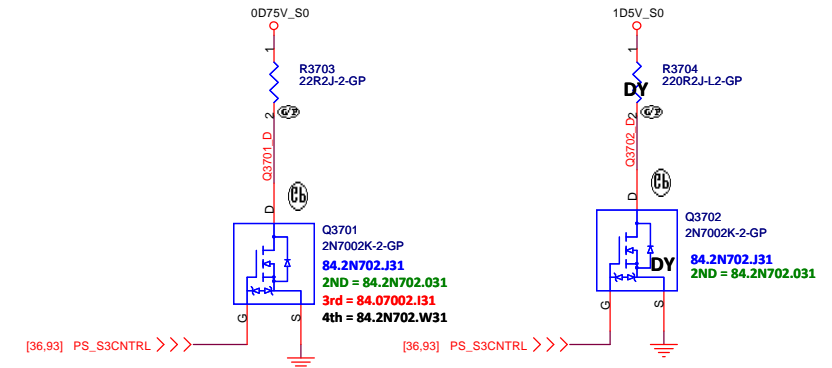
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



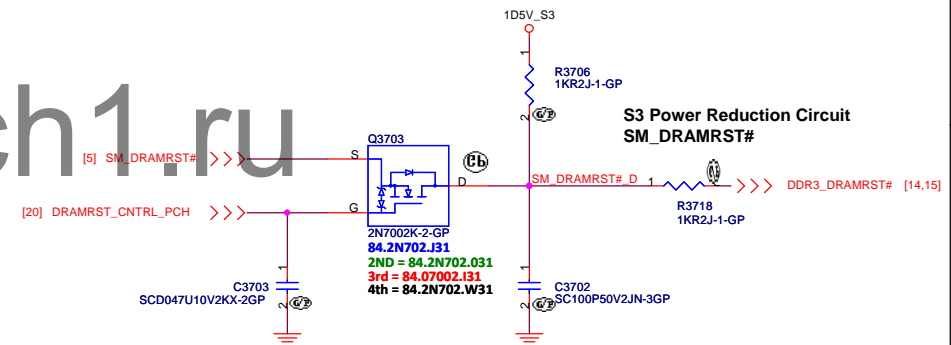
Close to CPU
S3 Power Reduction Circuit PM_DRAM_PWRGD



Close to DIMM
S3 Power Reduction Circuit PM_DRAM_PWRGD



Close to CPU
S3 Power Reduction Circuit SM_DRAMRST#



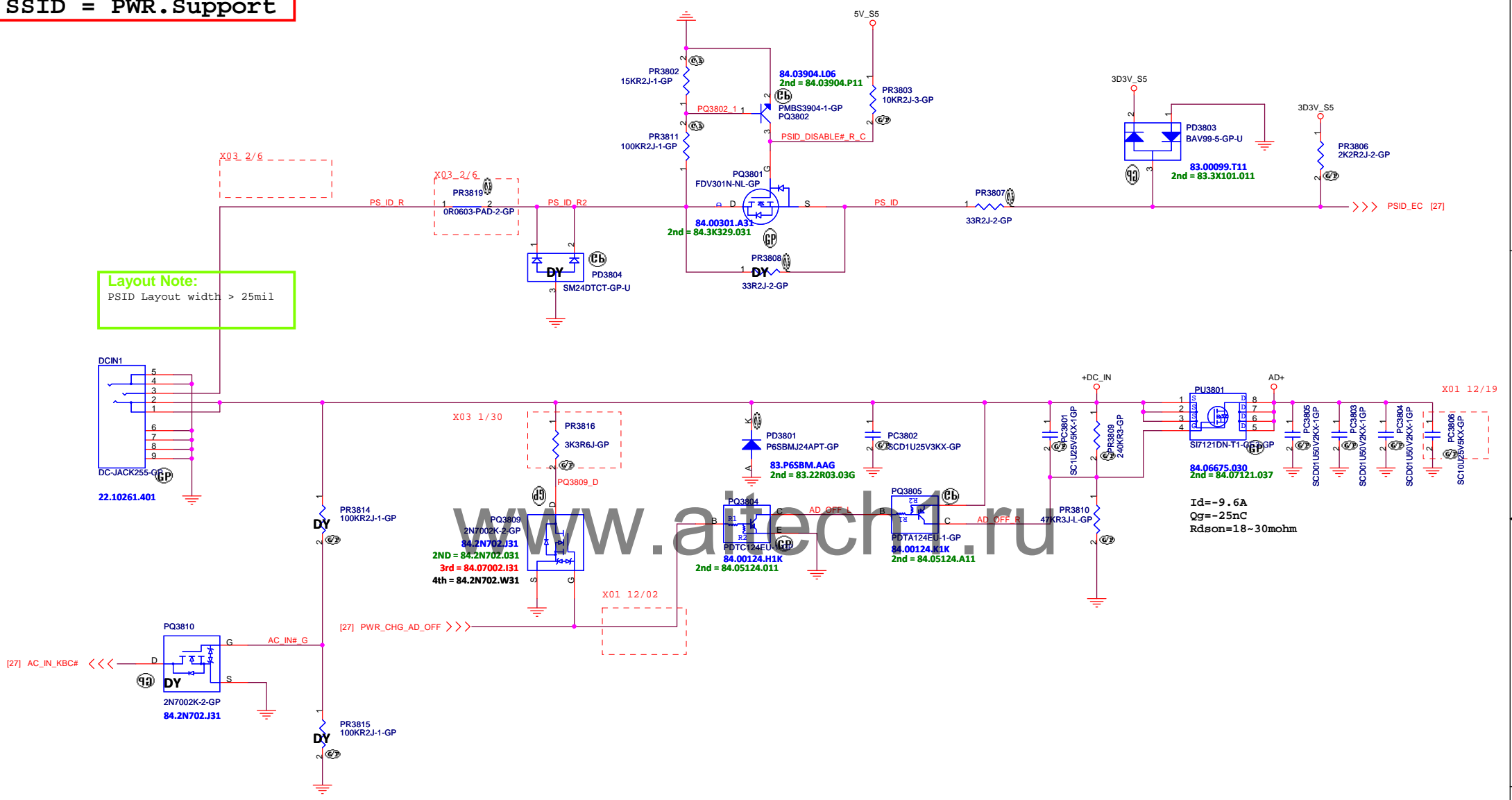
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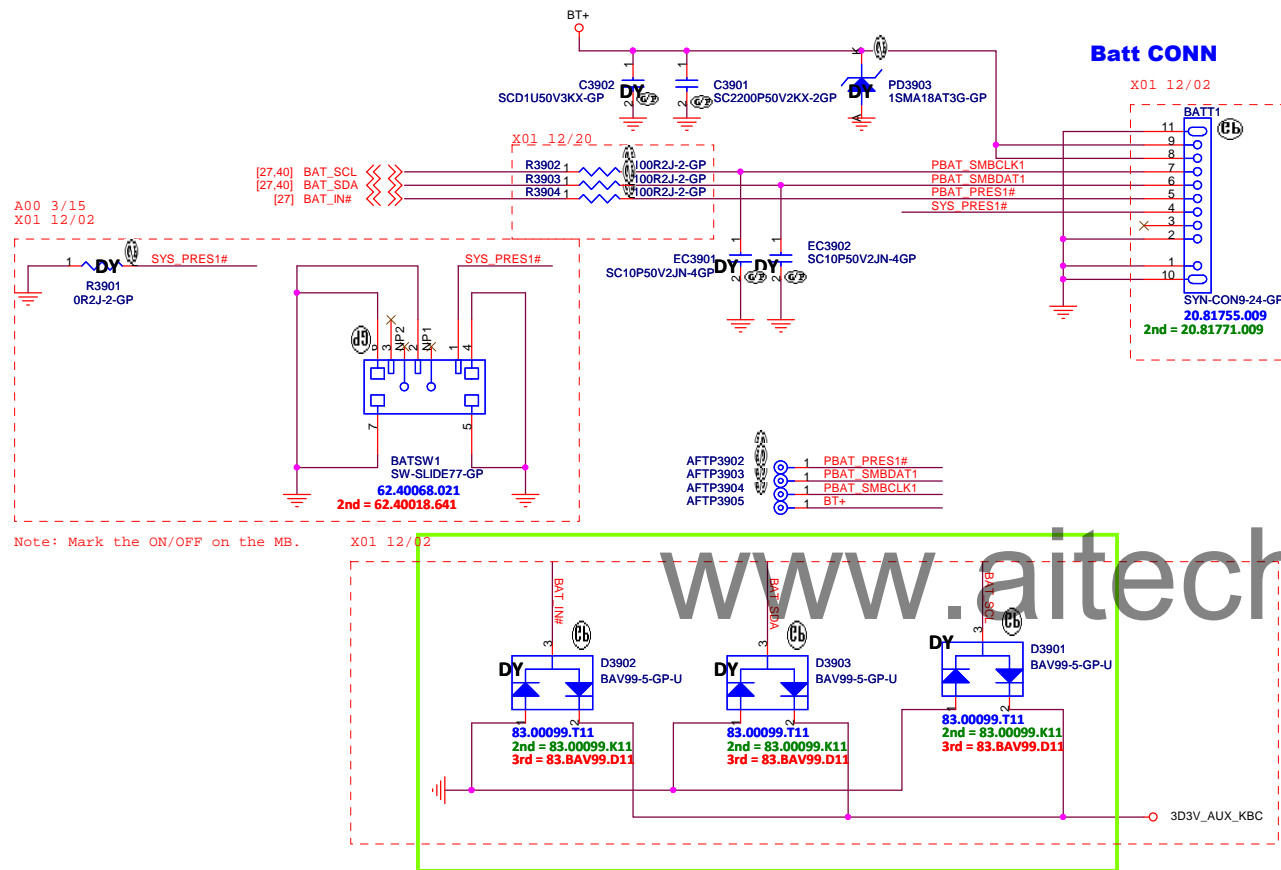
Title			S3 Power Reduction	
Size			Document Number	
A3			BMW Z4 DIS	
Date:			Friday, March 30, 2012	Sheet 37 of 105
Rev			A00	

```
SSID = PWR.Support
```



<Core Design>			
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Title			
		DCIN	
Size A3	Document Number	Rev	
	BMW Z4 DIS	A00	
Date:	Friday, March 30, 2012	Sheet	38 of 105
		1	

SSID = PWR.Support



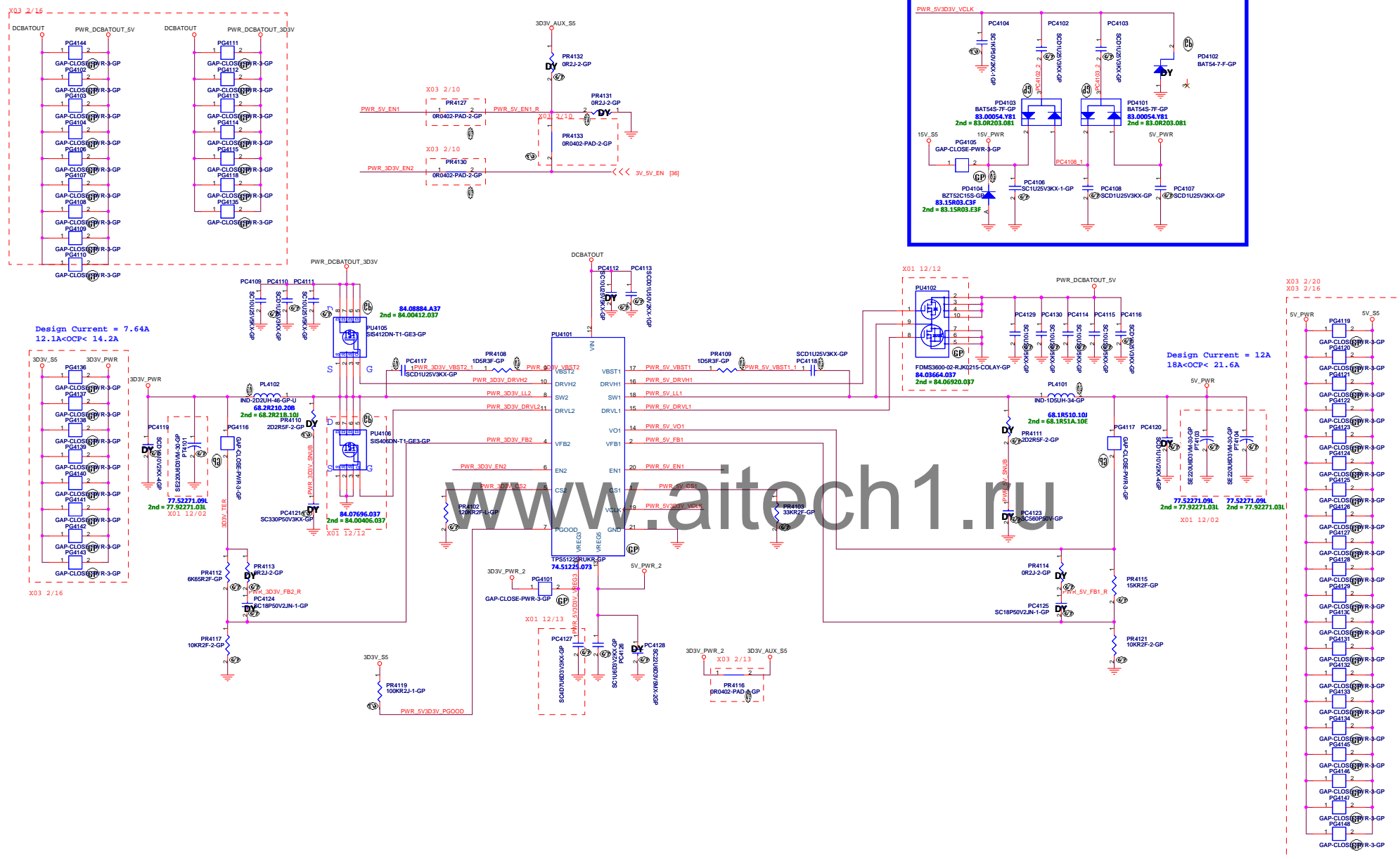
Layout Note:
Place near Battery CONN

<Core Design>

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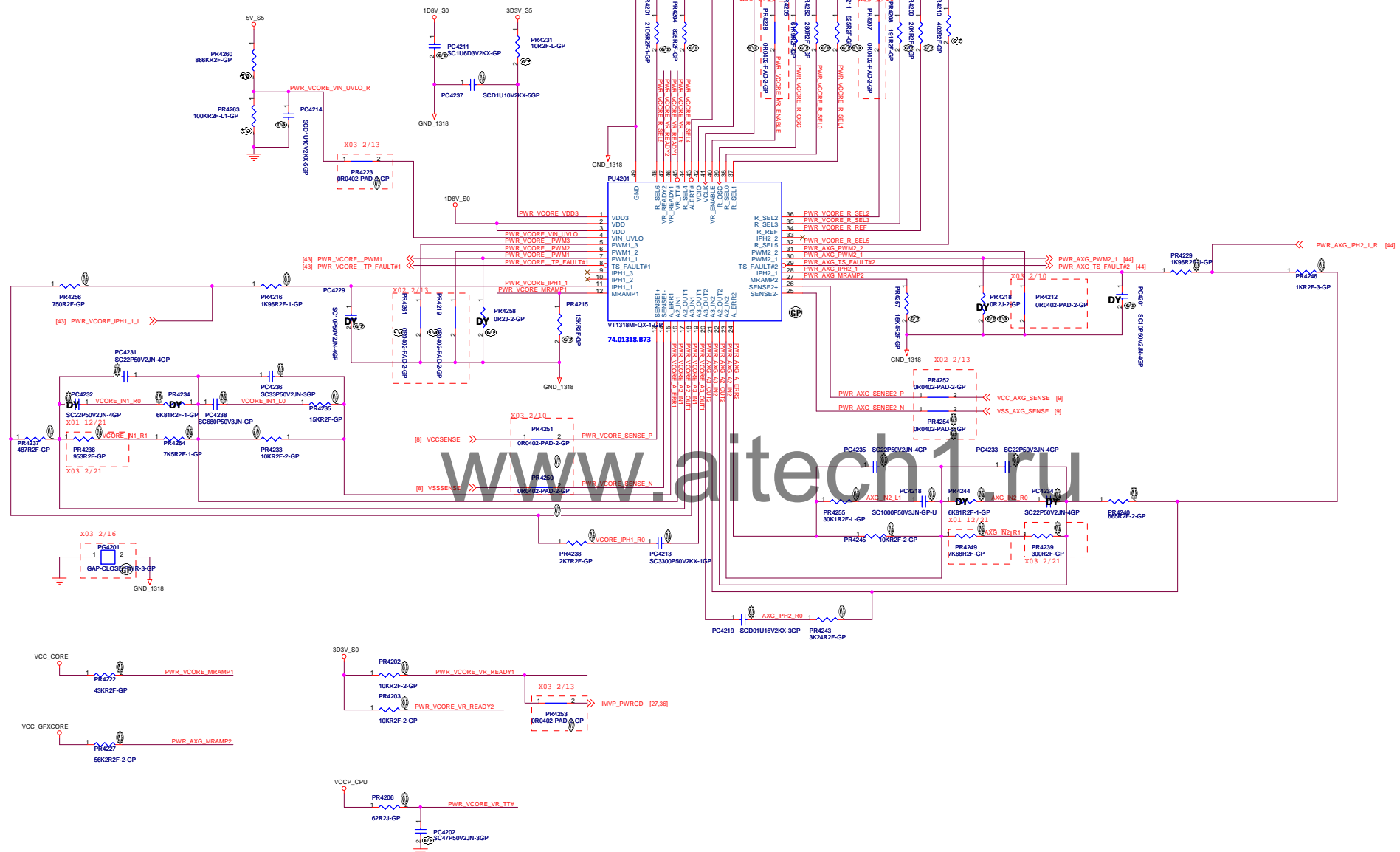
Title			BATT CONN	
Size	Document Number	Rev		
A3	BMW Z4 DIS	A00		
Date:	Friday, March 30, 2012	Sheet 39 of 105		


```
SSID = PWR.Plane.Regulator_5v3p3v
```



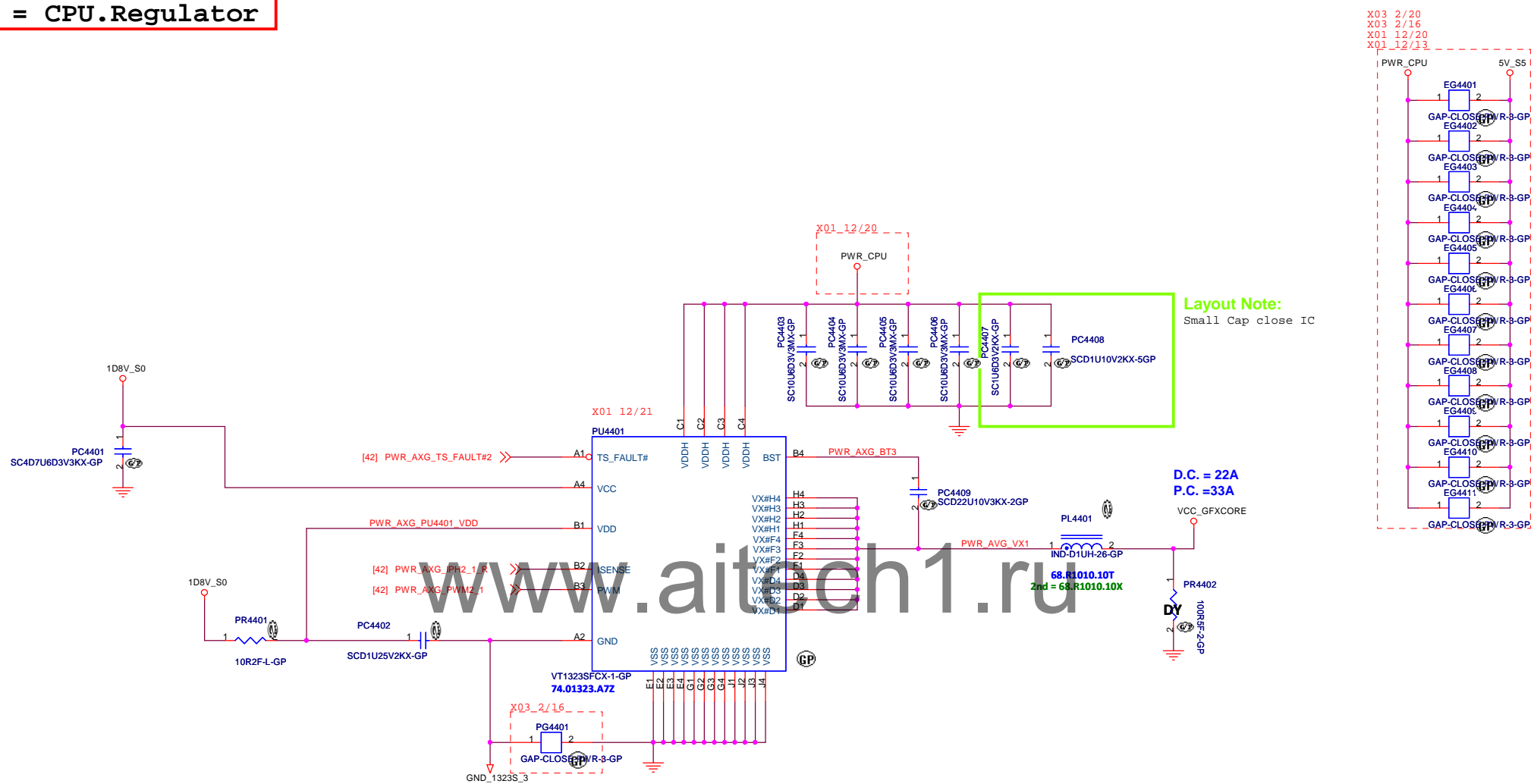
[8] VR_SVID_ALERT# <<< H_CPU_SVIDAT
 [8] H_CPU_SVIDDAT >>> H_CPU_SVIDAT
 [8] H_CPU_SVIDCLK >>> H_CPU_SVIDCLK
 [48] DB5V_PWRGD >>> boot voltage=0V

Volterra's suggestion:
 VCC 26x22uF(0805) 1-PHASE VCC
 VCCAXG 23x22uF(0805) for 1-PHASE VCCAXG

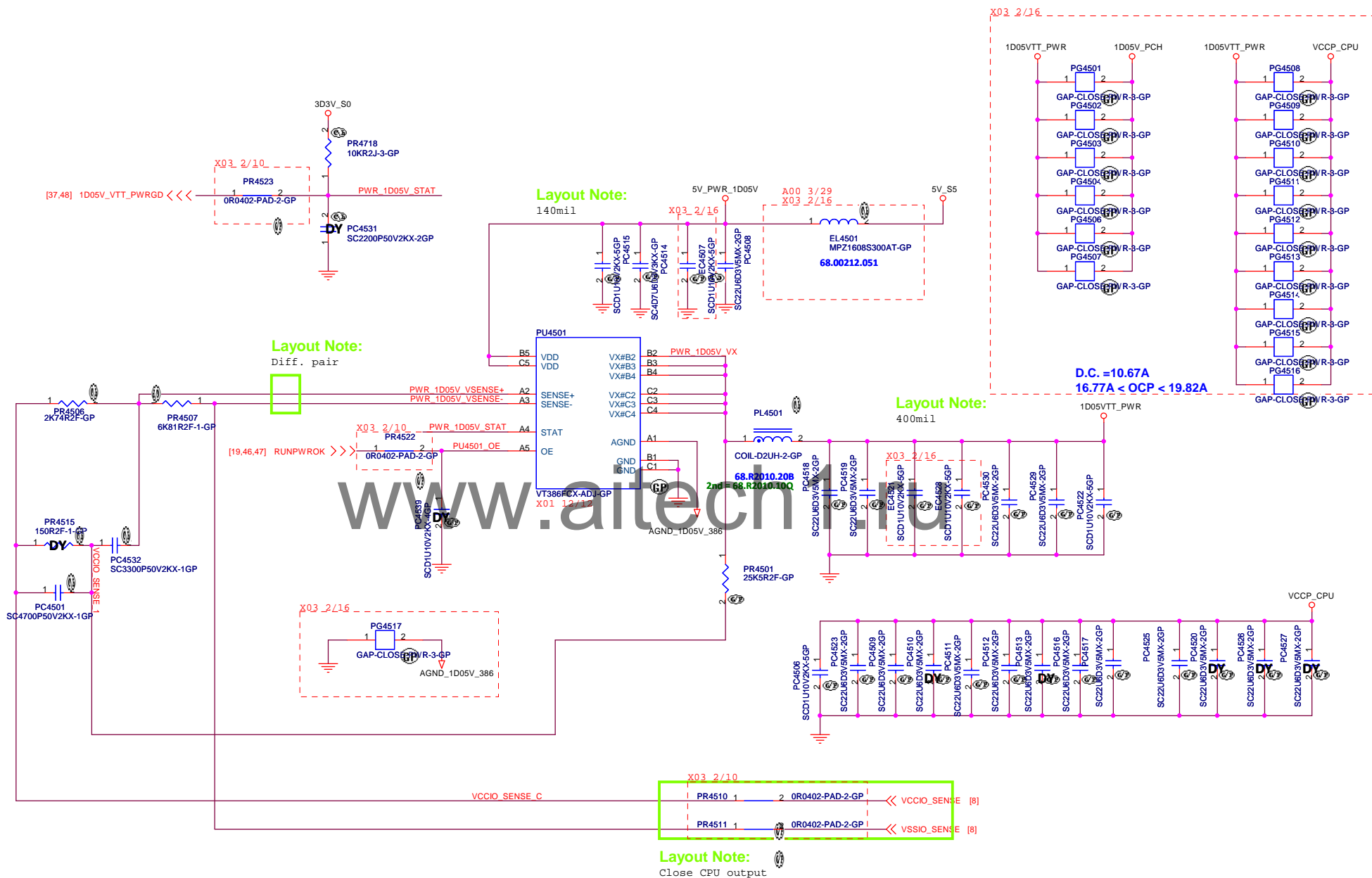


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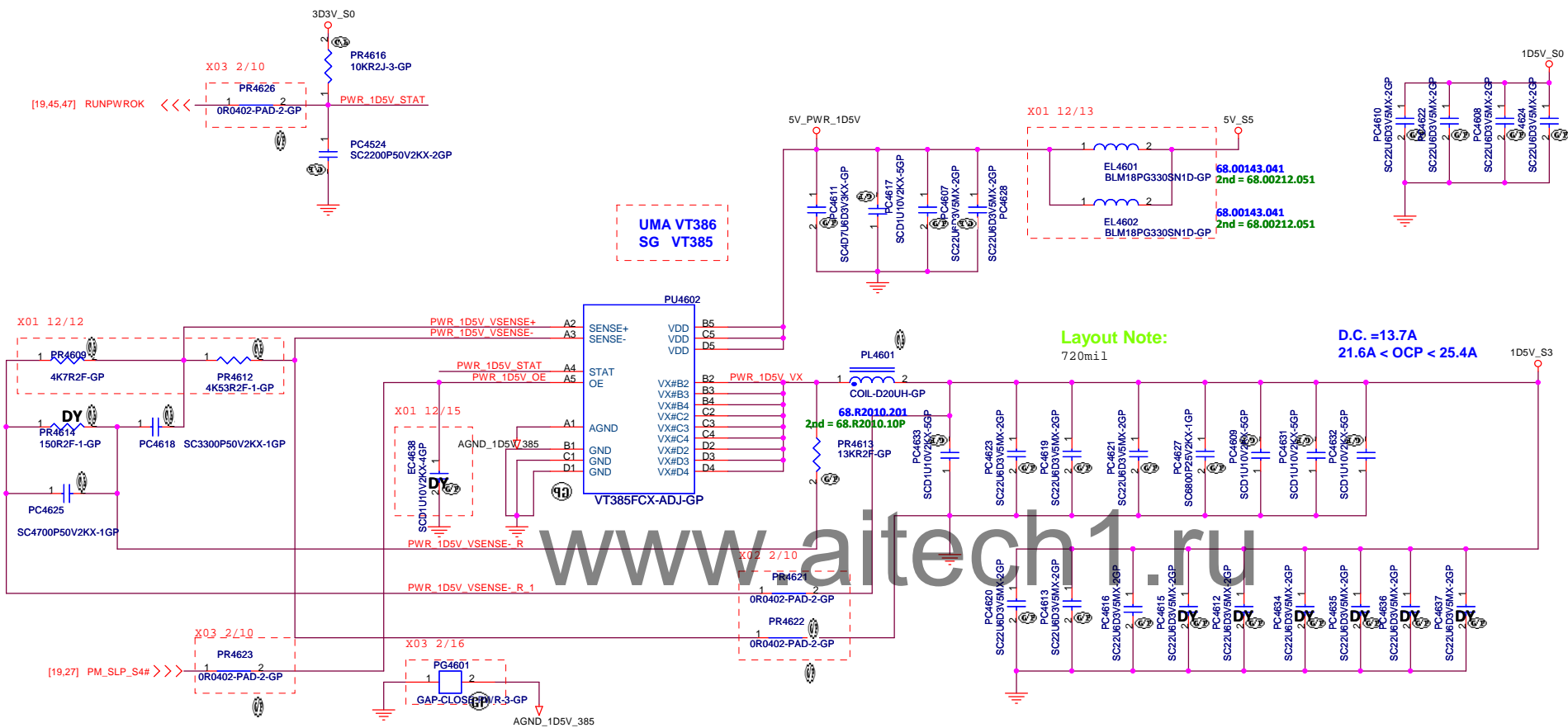

```
SSID = CPU.Regulator
```



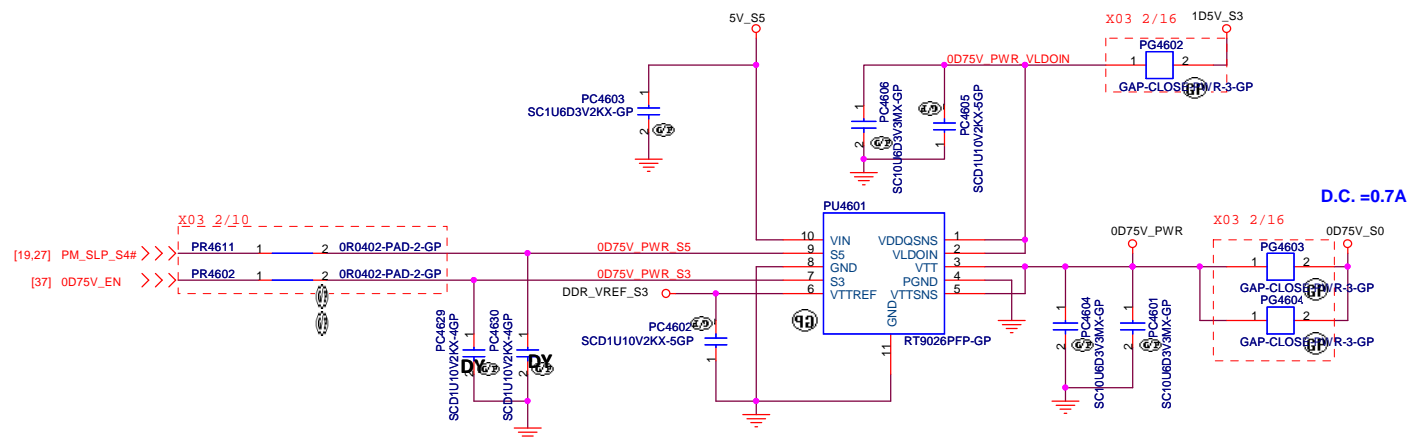
SSID = PWR.Plane.Regulator_1p05v



```
SSID = PWR.Plane.Regulator_1p5v0p75v
```



RT9026 for 0D75V_S0



<Core Design>

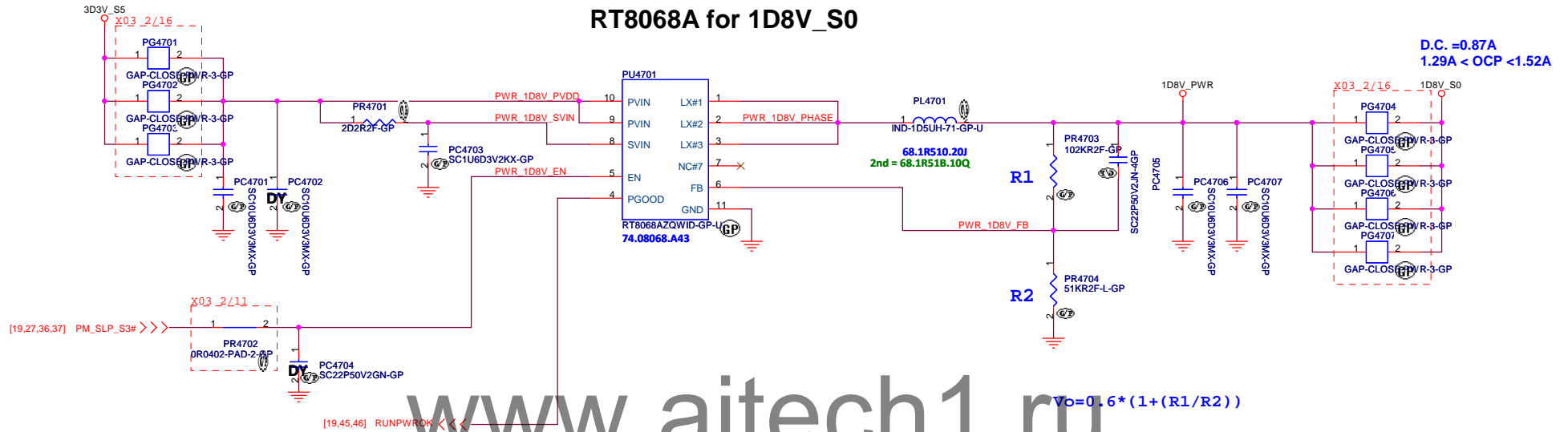


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Title			
VT385 1D5V S3/RT9026 0D75V S0			
Size A3	Document Number	Rev	
	BMW Z4 DIS	A00	
Date:	Friday, March 30, 2012	Sheet 46 of	105

SSID = PWR.Plane.Regulator_1p8v

RT8068A for 1D8V_S0



<Core Design>

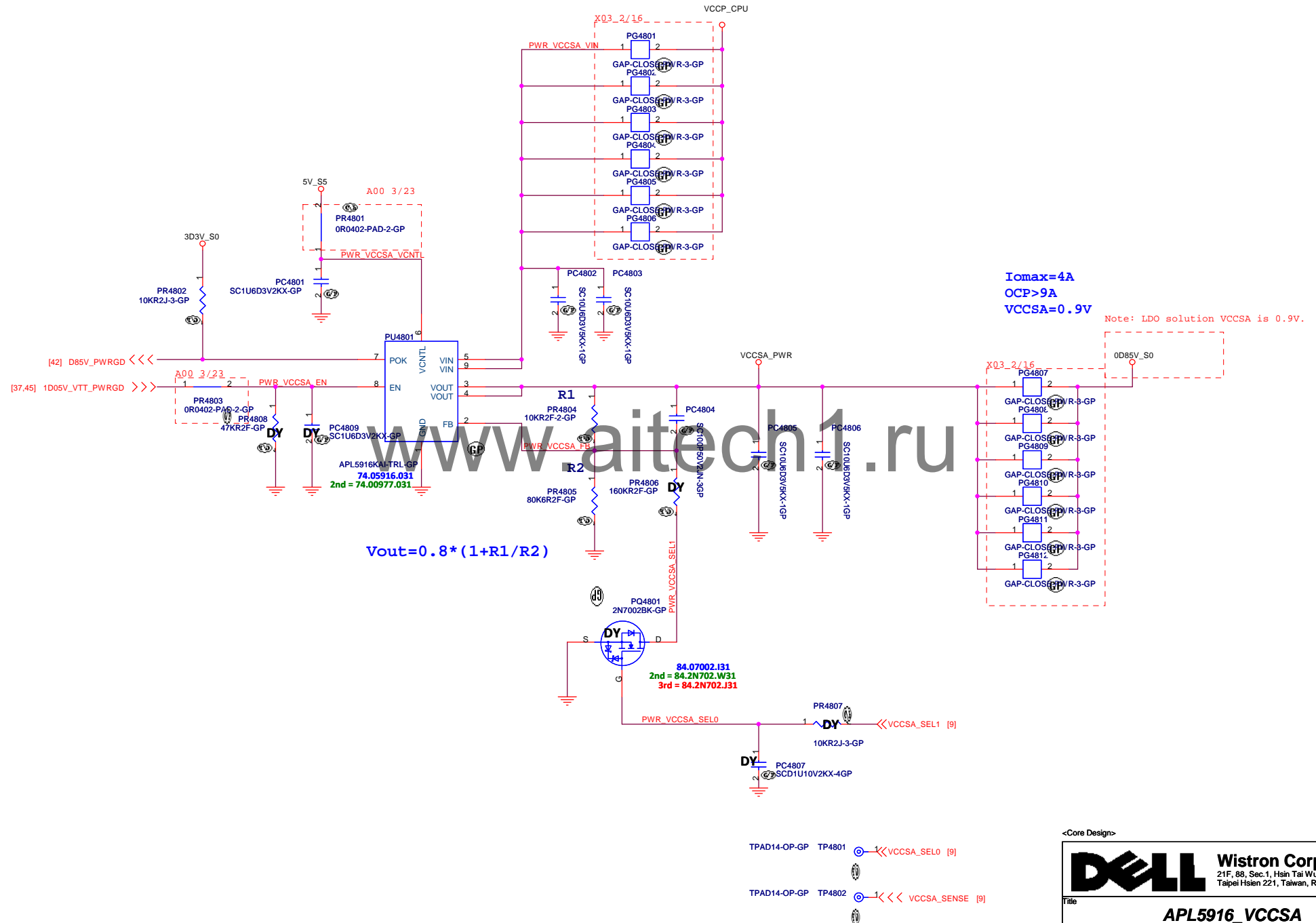


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Title			RT8068A 1D8V S0	
Size	Document Number	Rev		A00
A3	BMW Z4 DIS			
Date:	Friday, March 30, 2012	Sheet	47	of 105

SSID = PWR.Plane.Regulator_vccsa

X02 1/9



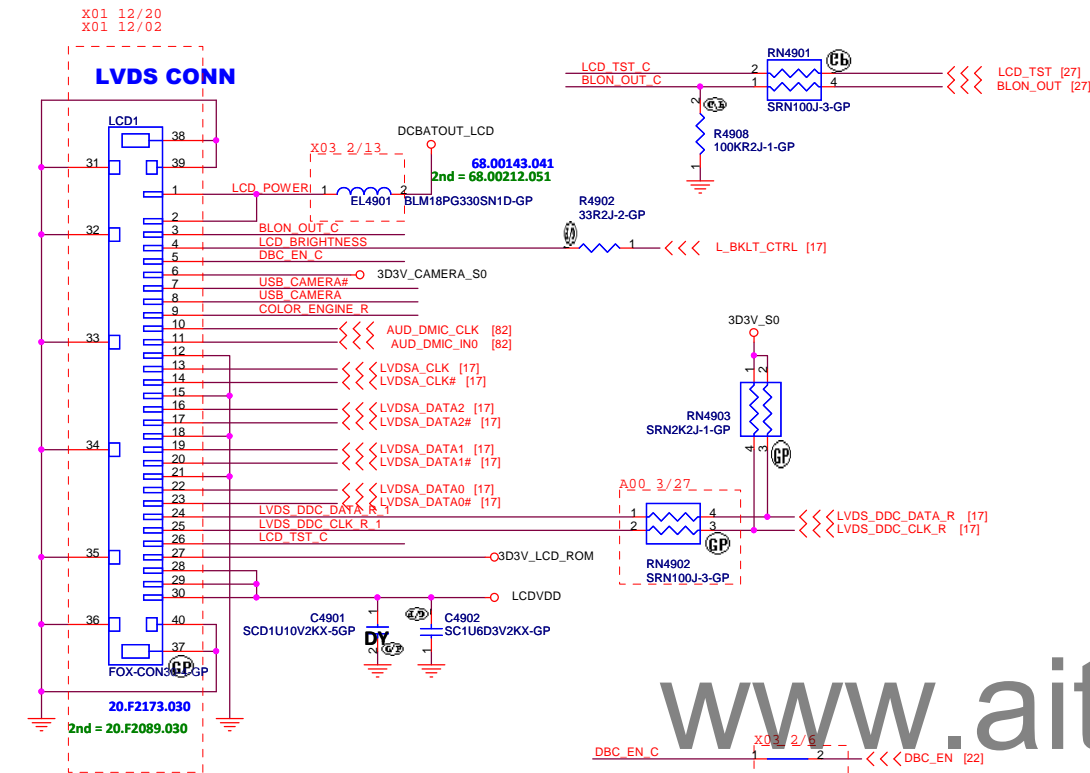
<Core Design>



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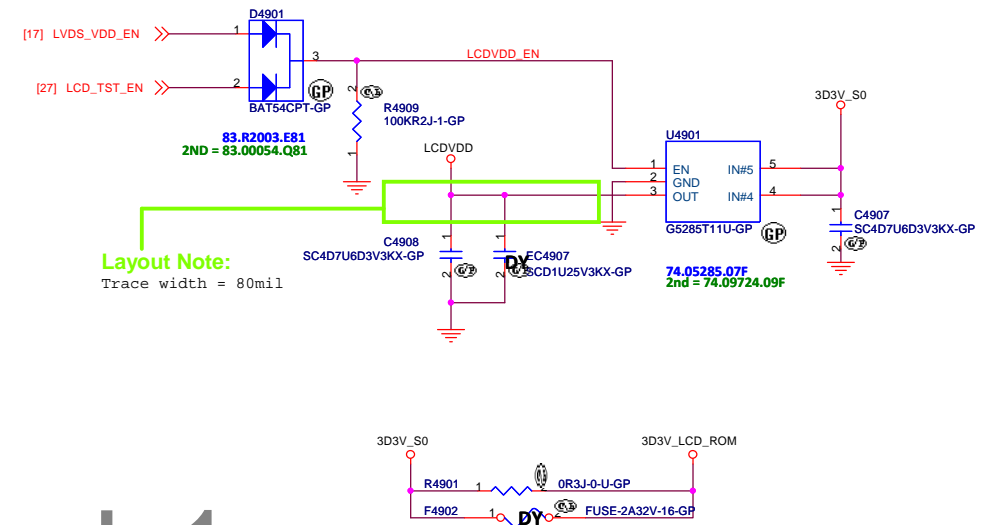
Title			APL5916 VCCSA	
Size	Document Number	Rev		
A3	BMW Z4 DIS	A00		
Date:	Friday, March 30, 2012	Sheet	48	of 105

SSID = VIDEO

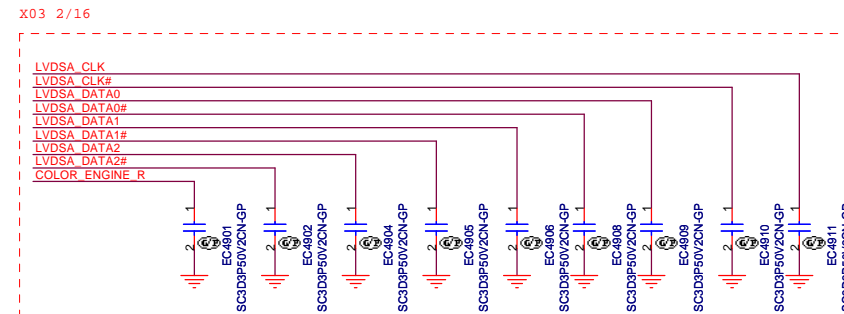


SSID = VIDEO

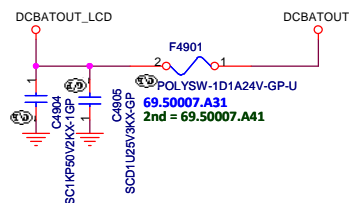
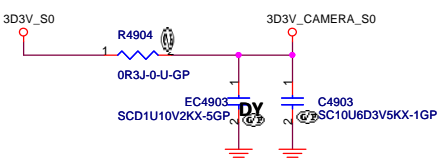
LCD Power for ROSA



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Camera Power




<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>LCD Connector</i>			
Size A3	Document Number		Rev <i>A0</i>
<i>BMW Z4 DIS</i>			
Date: Tuesday, April 03, 2012	Sheet 49		of 105

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Title

CRT Connector

Size
A3

Document Number
BMW Z4 DIS

Date: Friday, March 30, 2012

Rev
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HDMI Level Shifter



Title			
HDMI Level Shifter/Connector			
Size A3	Document Number	Rev	
	BMW Z4 DIS	A00	
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Title

Reserved

Size
A3

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Date: Friday, March 30, 2012

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Document Number

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Date: Friday, March 30, 2012

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Title

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Size
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Document Number
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Date: Friday, March 30, 2012

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Title

ITP/Fan Connector

Size
A3

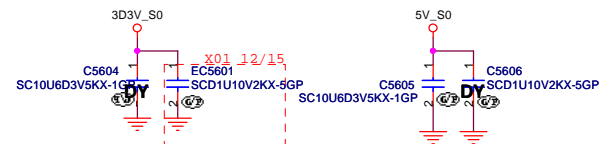
Document Number
BMW Z4 DIS

Rev
A00

Date: Friday, March 30, 2012

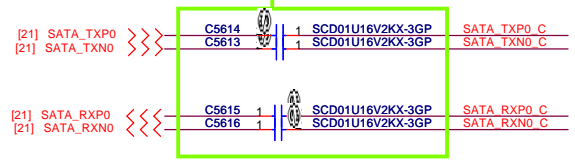
Sheet 55 of 105

SSID = SATA

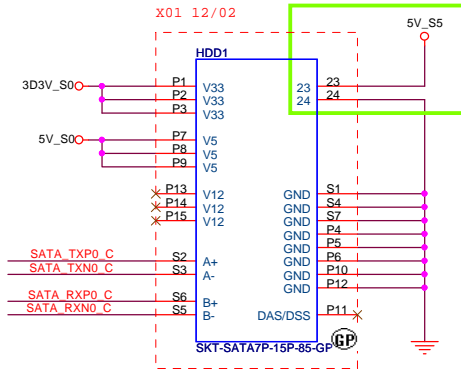


Layout Note:

AC coupling Cap;
place near CONN(<100mils)



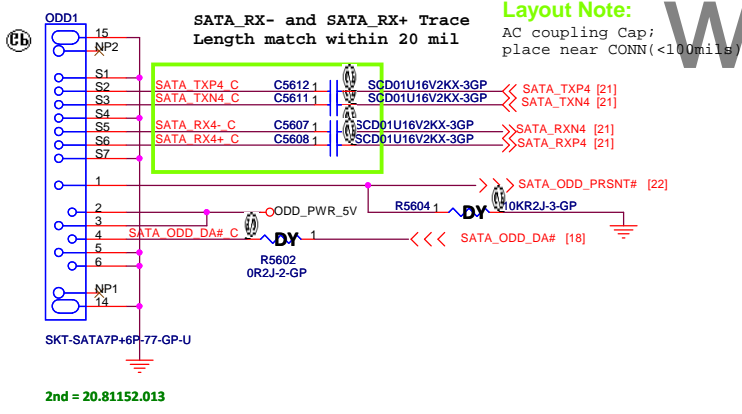
HDD CONN



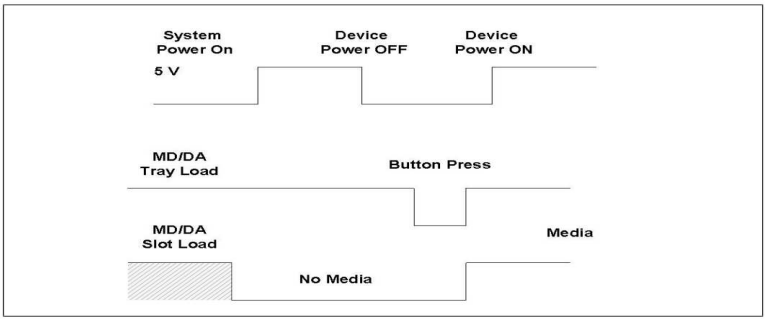
Due to layout, HDD1 pin 23 modify 5V_S5

20.81599.022
2nd = 22.10300.C51

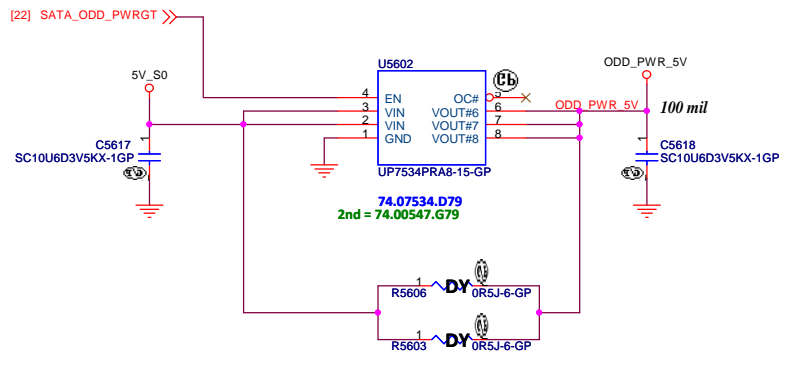
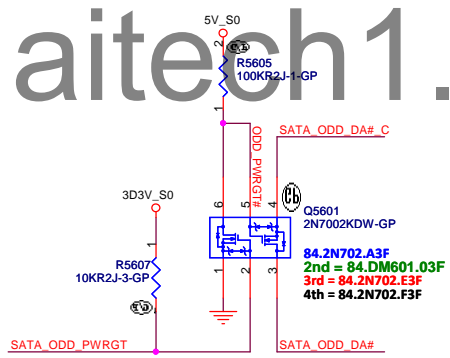
ODD CONN



Zero Power ODD Power Sequence



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Title HDD/ODD		
Size A3	Document Number BMW Z4 DIS	Rev A00
Date: Friday, March 30, 2012	Sheet 56	of 105

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Title			
Reserved			
Size A3	Document Number BMW Z4 DIS		Rev A00
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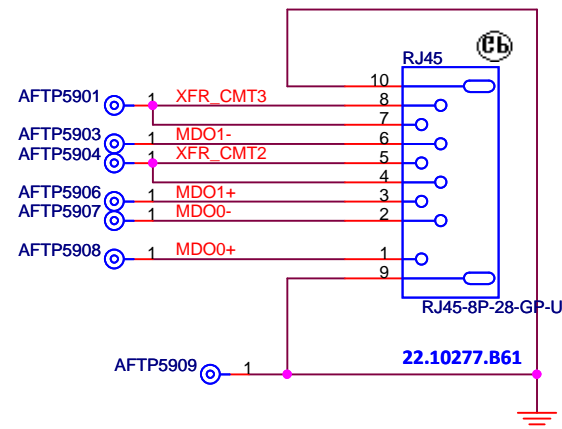
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SSID = LOM



RJ45 Connector



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[illegible]

RJ45+Transfermer

Size
A4

Document Number	
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BMW Z4 DIS

Rev

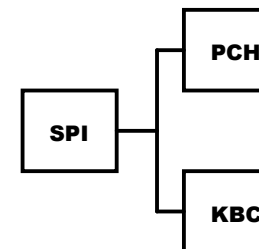
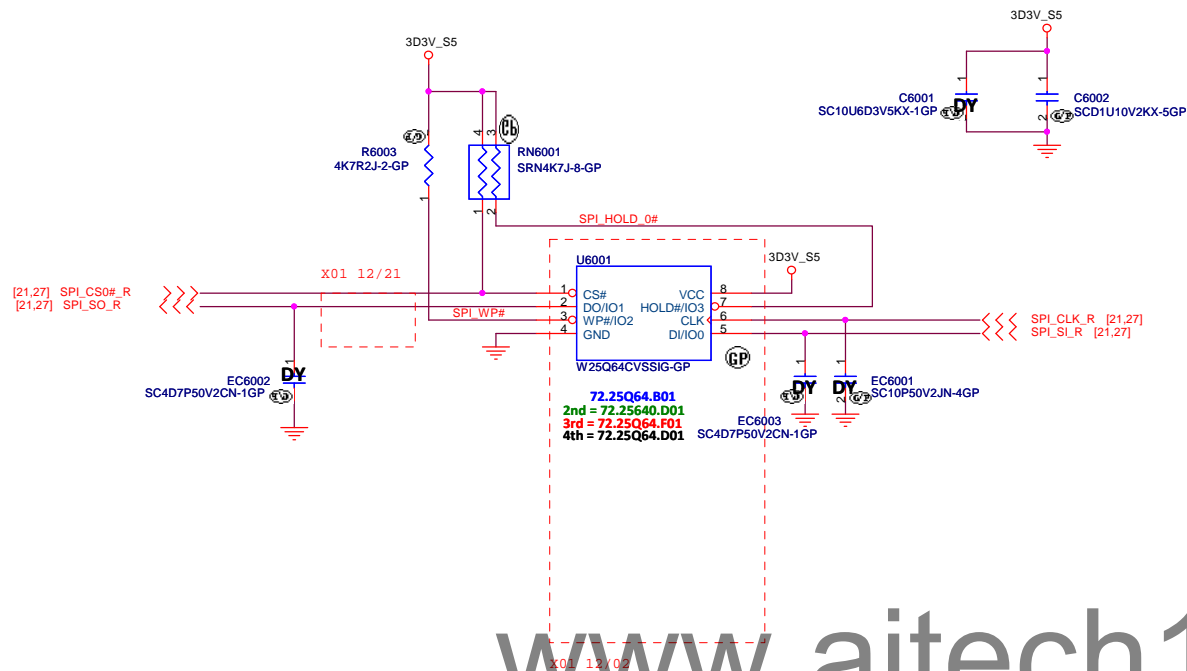
Date: Tuesday, April 03, 2012

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AOC

SSID = Flash.ROM

SPI Flash ROM(8M) for PCH

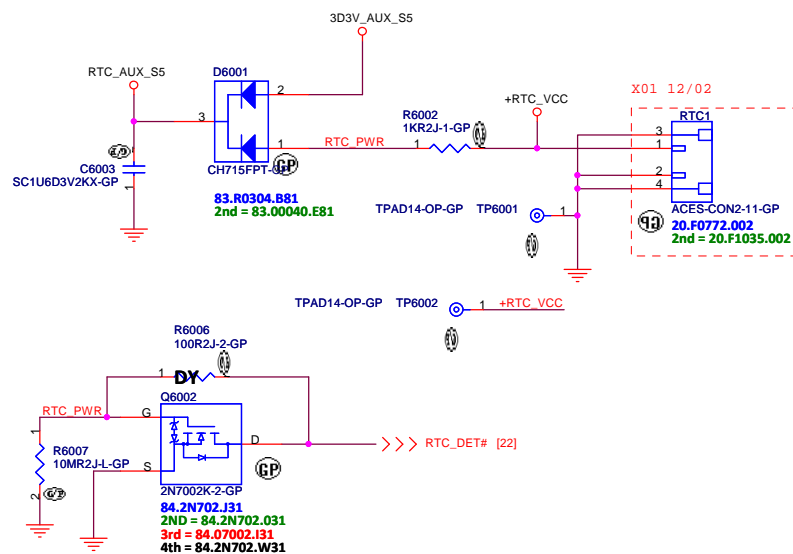


Layout Note:

KBC---10"---PCH
KBC---1.5"~6.5"---SPI
PCH---0.5"~6.5"---SPI

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SSID = RBATT



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Title

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SizeDocument Number

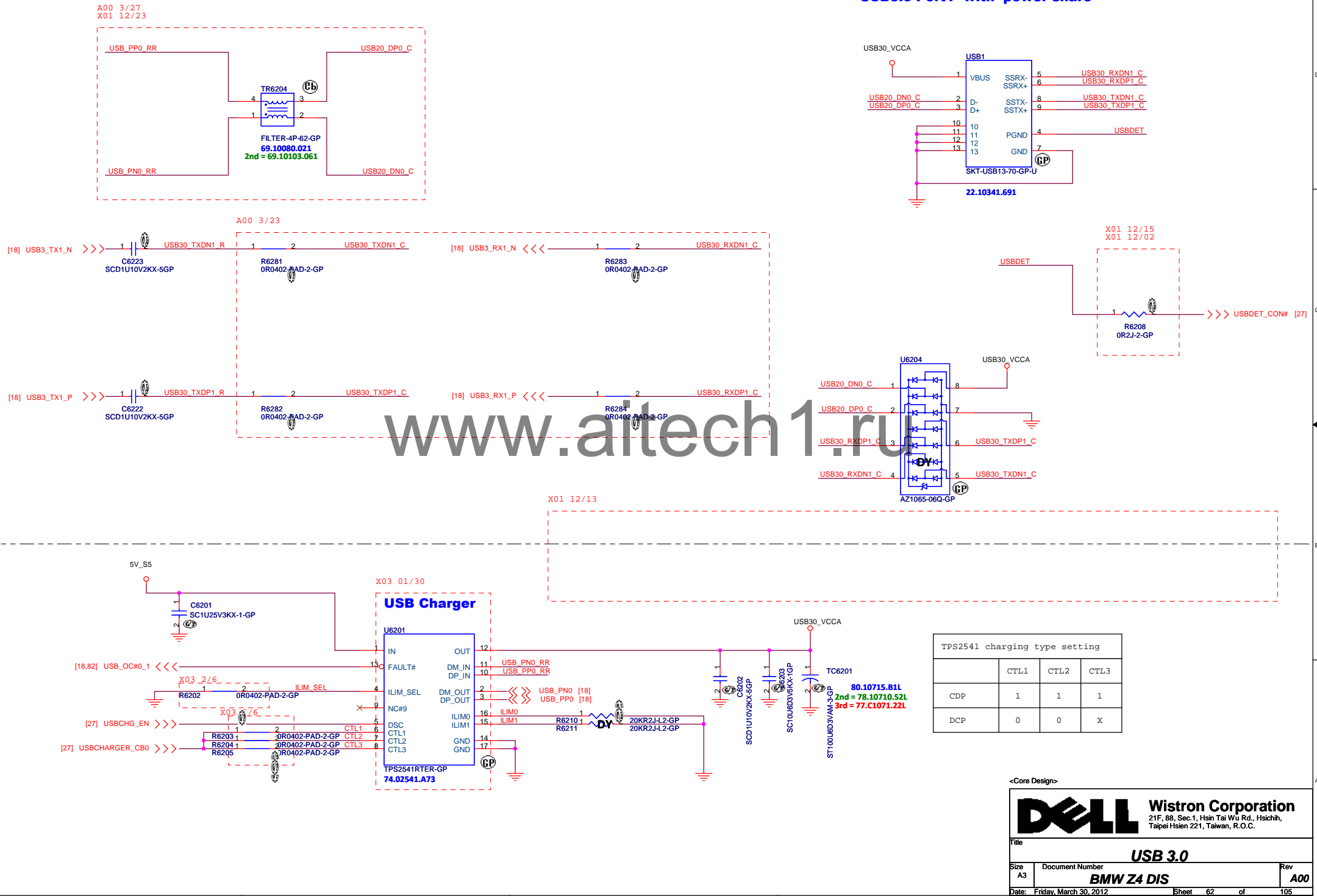
Rev

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SSID = USB

USB3.0 Port1 with power share



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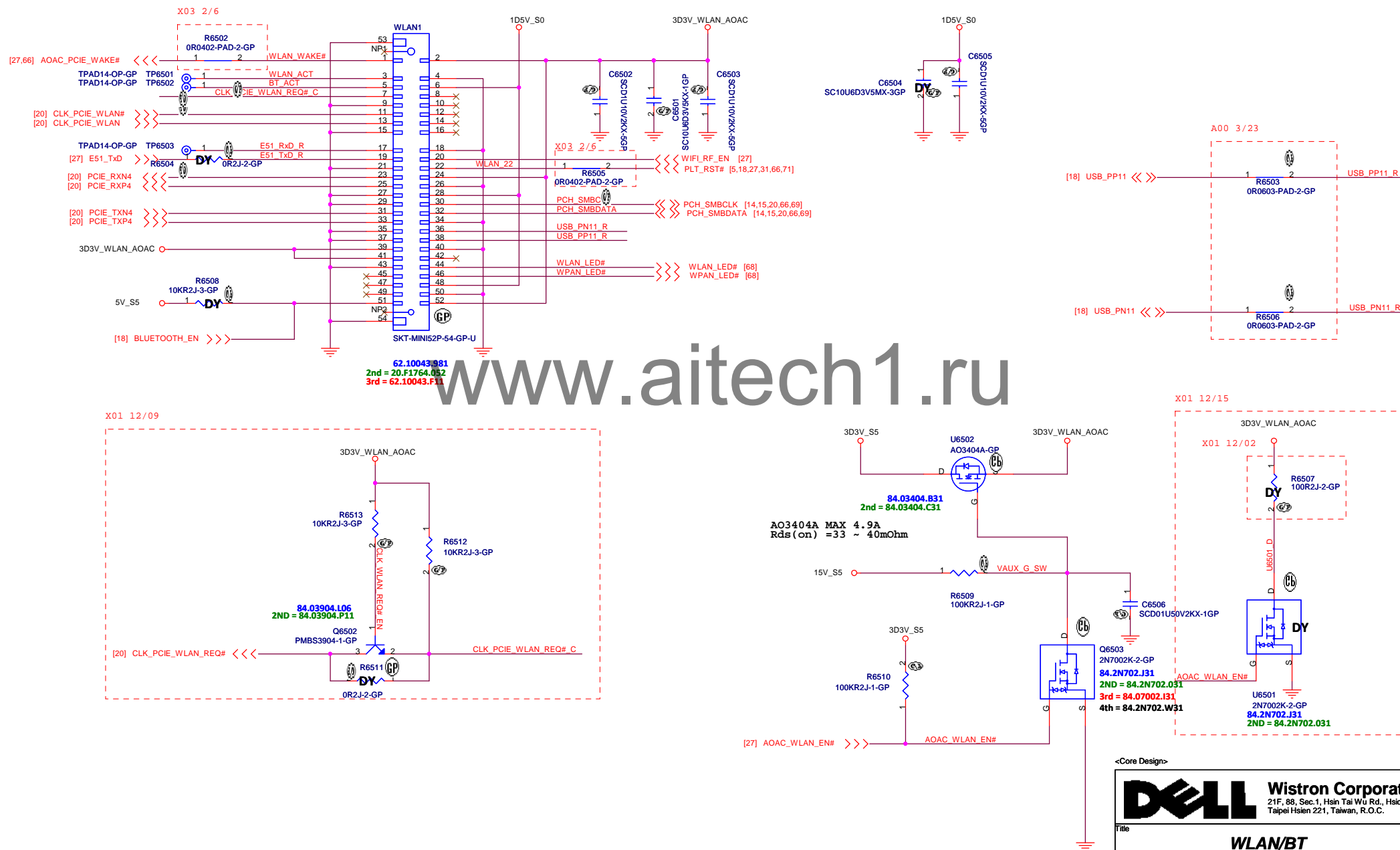
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Finger Printer			
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SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

WLAN CONN

<Core Design>

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WLAN/BT


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A3	BMV71-B10	

RS	BMW Z4 DIS	A
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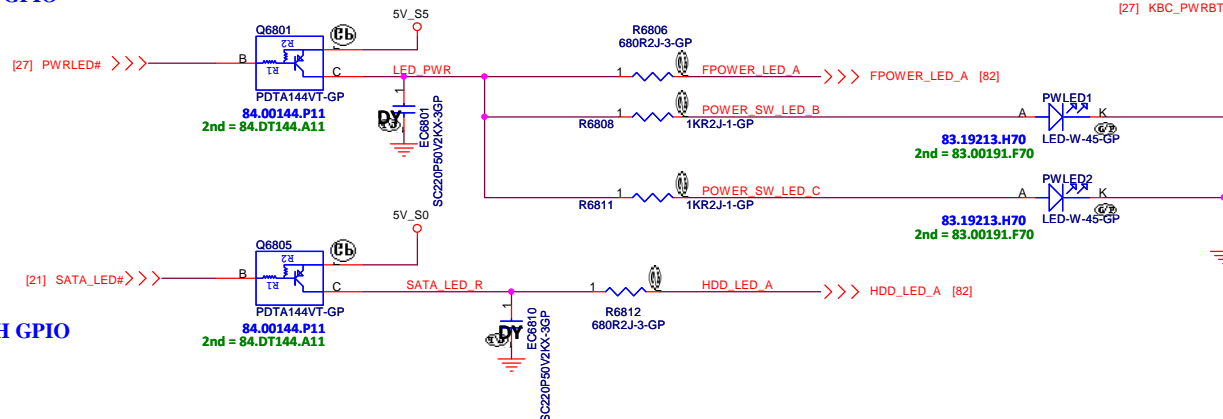
Date: Friday, March 30, 2012

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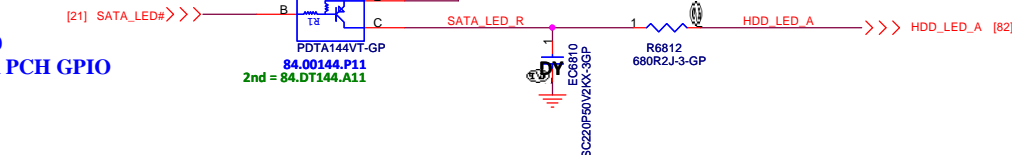
SSID = User.Interface

Front Power LED

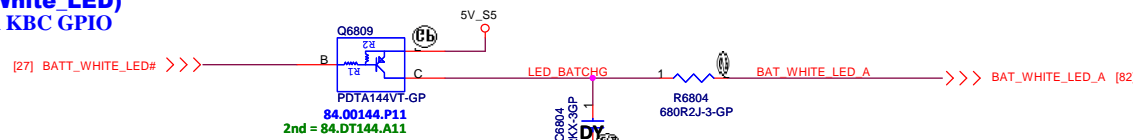
LOW actived from KBC GPIO



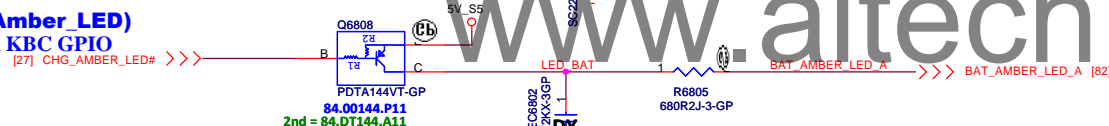
SATA HDD LED
LOW actived from PCH GPIO



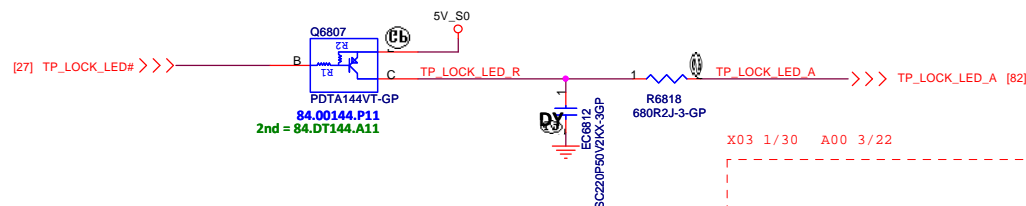
Battery LED2(White_LED)
LOW actived from KBC GPIO



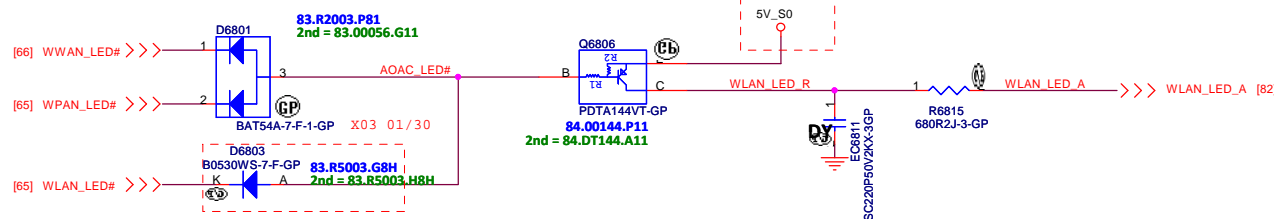
Battery LED1(Amber_LED)
LOW acted from KBC GPIO



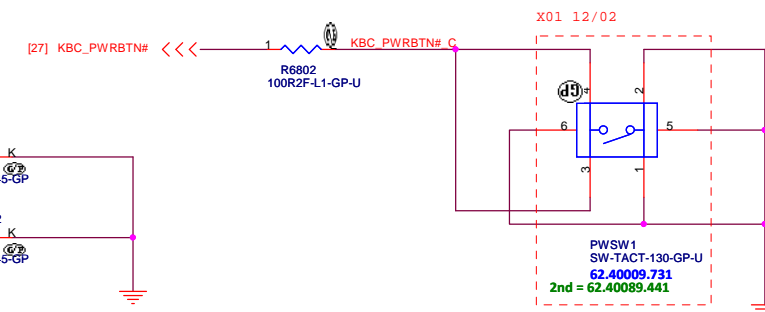
TPLOCK LED
LOW actived from KBC GPIO



WLAN LED
LOW actived from KBC GPIO



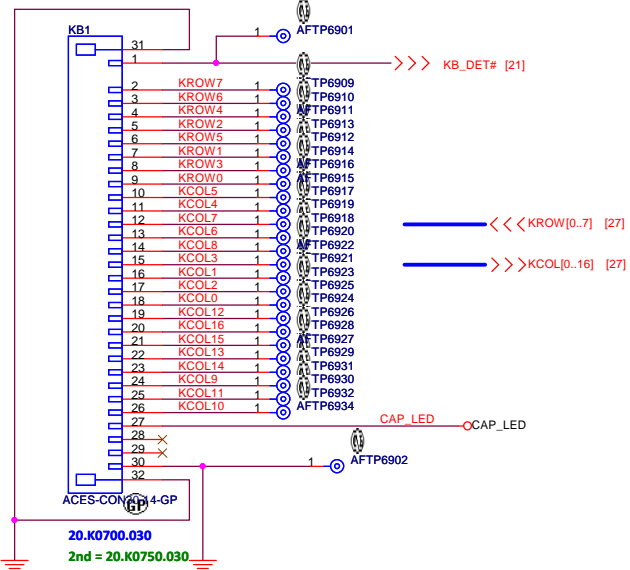
PWRBTN



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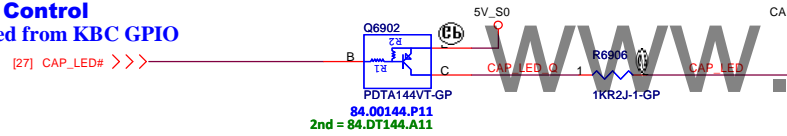
SSID = KBC

Internal Keyboard Connector



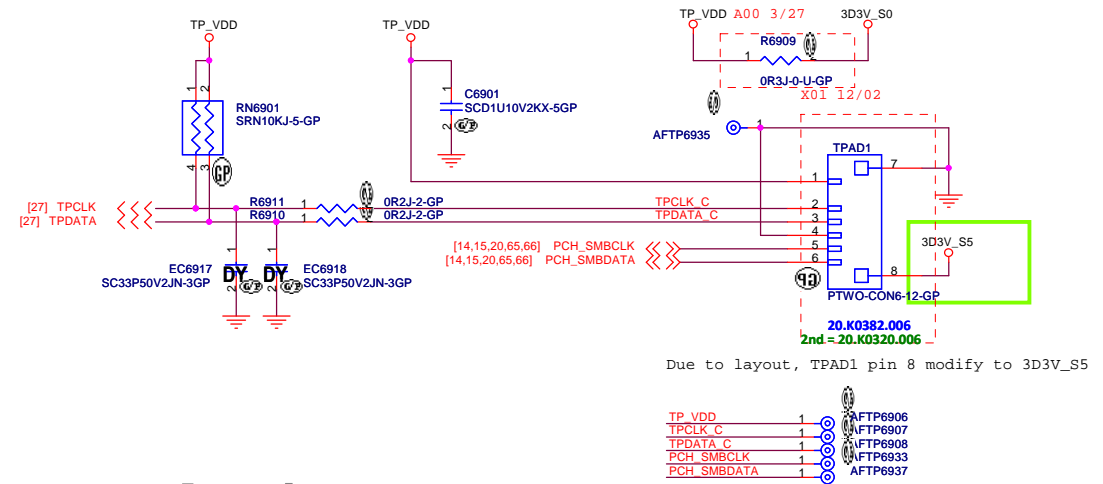
CAP LED Control

LOW acted from KBC GPIO



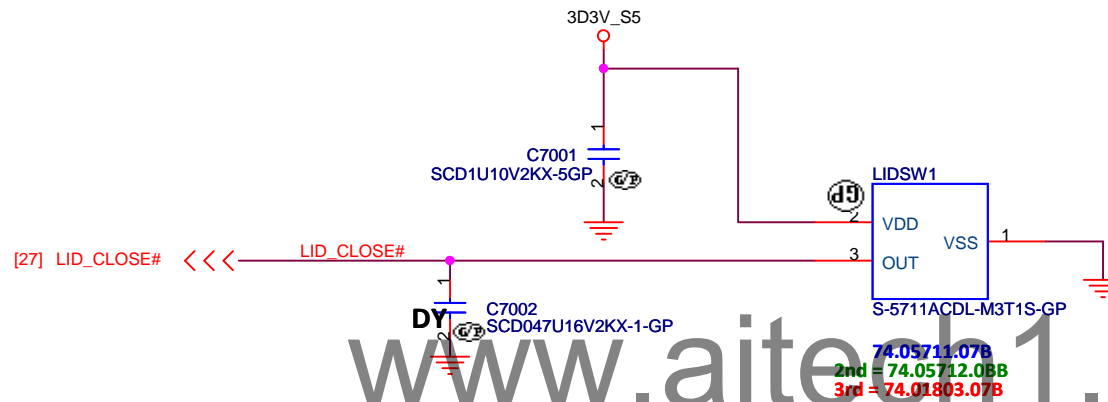
SSID = Touch.Pad

Touch Pad Connector



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SSID = User.Interface



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Hall Sensor

Size
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Document Number

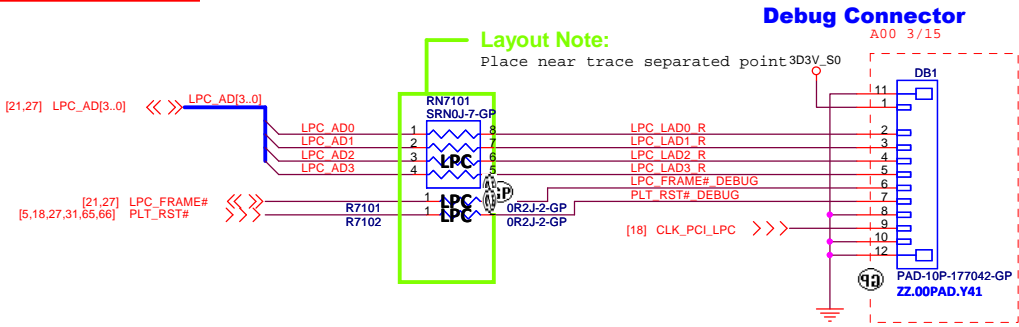
BMW Z4 DIS

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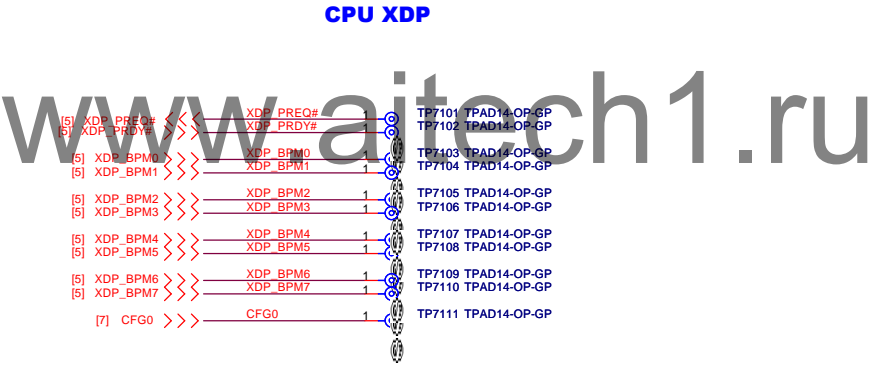
Date: Friday, March 30, 2012

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SSID = DEBUG PORT



SSID = CPU



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Size
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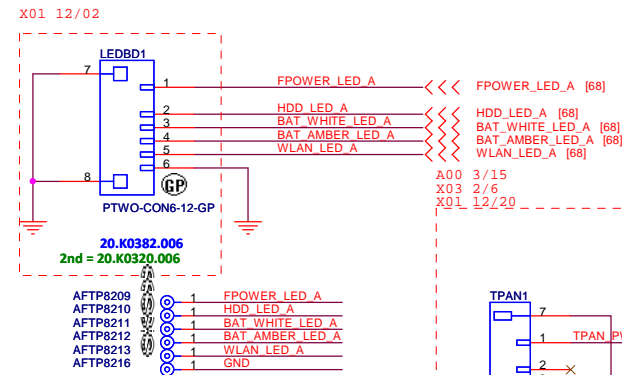
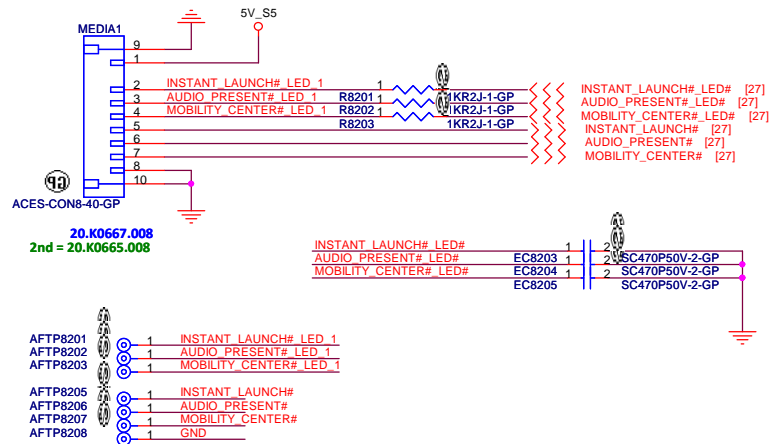
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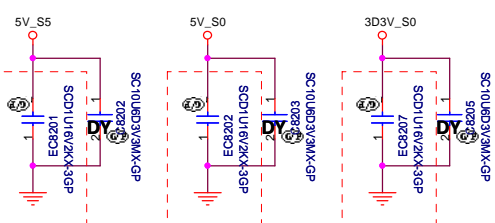
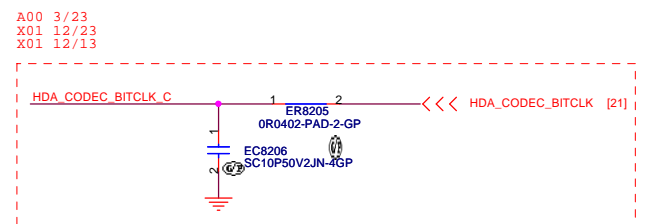
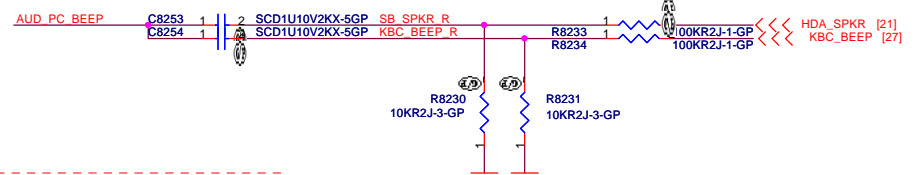
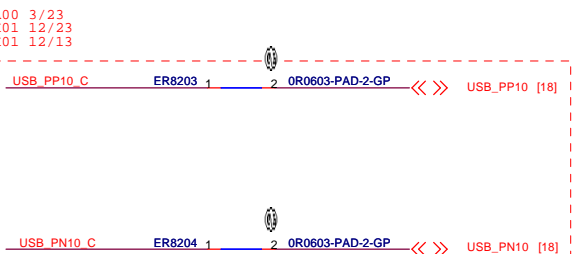
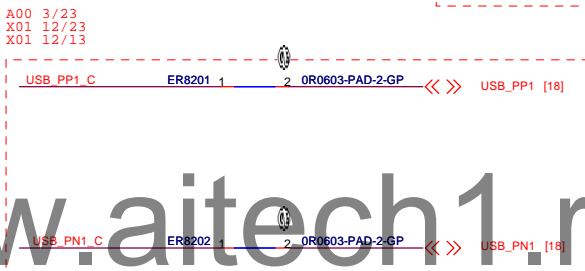
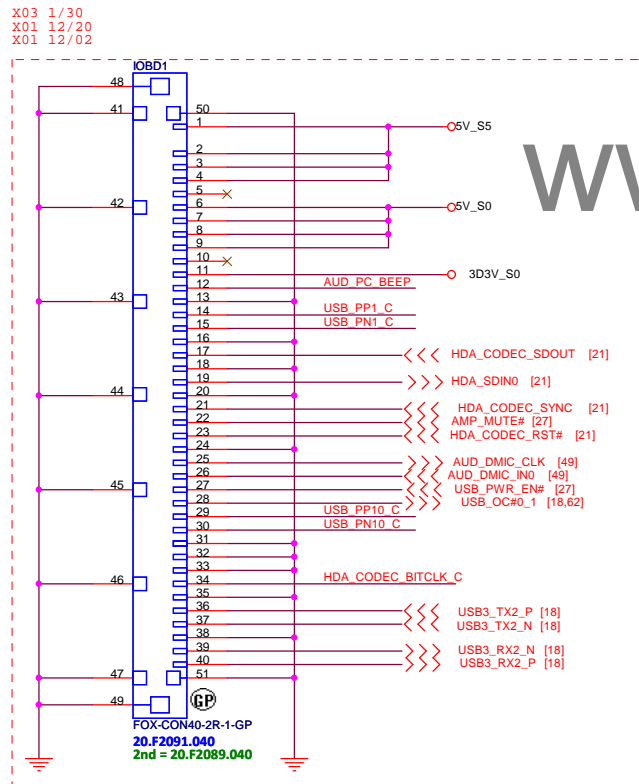
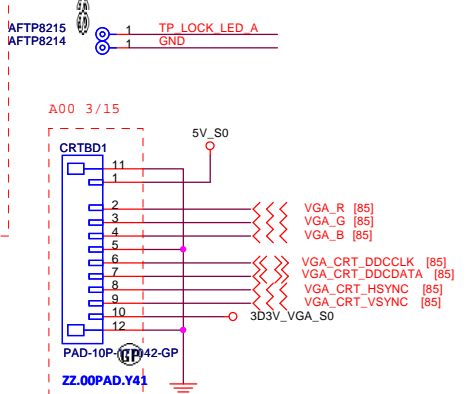
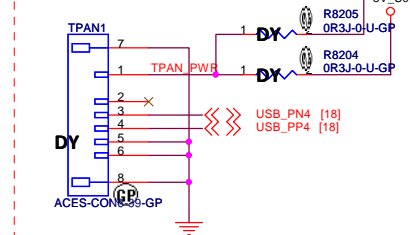
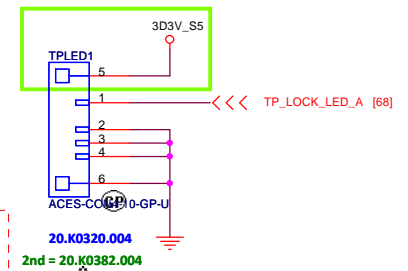
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SSID = User.Interface



Due to layout, TPLED1 pin 5 modify 3D3V_S5



X01 12/09 Request by EMI

A00 3/27

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Title: **IO Board Connector**

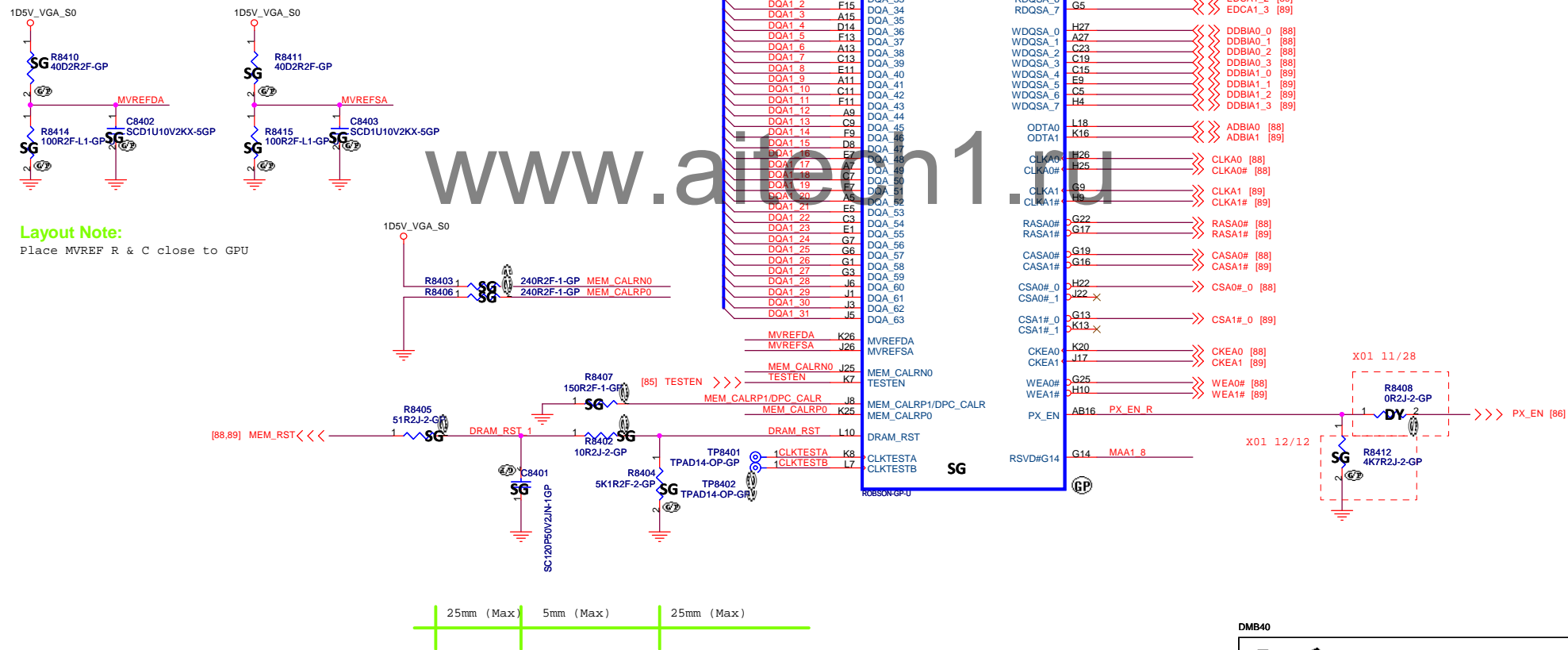
Size: A3 Document Number: **BMW Z4 DIS** Rev: **A00**

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SSID = VIDEO



SSID = VIDEO



Layout Note:

Place all these components very close to GPU
(Within 25mm) and keep all component close
to each Other (within 5mm) except R_MEM_2

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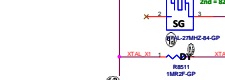
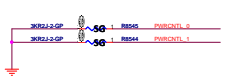
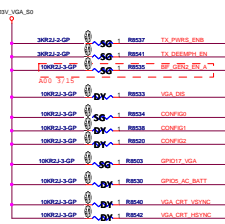


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Title			GPU Memory(2/5)	
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CONFIGURATION STRAPS				
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED	PLATFORM RESET
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0: Advertises the PCIe device as 2.50G/s capable at power on 1: Advertises the PCIe device as 5.00G/s capable at power on	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low	?	0
GPIO8_ROMSO	GPIO8	0: VGA Controller capacity enabled 1: The device won't be recognized as the system's VGA controller	0	0
VGA_DIS	GPIO9	0: Disable external BIOS ROM device 1: Enable external BIOS ROM device	0	0
ROMIDCFG2_0	GPIO[13:11]	BIOS ROM ID Config2 defines the ROM type BIOS_ROM_0h, BIOS_ROM_1h, BIOS_ROM_2h defines the primary memory aperture size	X X X	0 0 1 (2 5 0 0 0 1)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO22_ROMCEN	0: Disable external BIOS ROM device 1: Enable external BIOS ROM device	X	0
VP_DEVICE_STRAP_IN	V2SYNC	VP Device Strap Enable Indicate to the software driver that it sense whether or not a VP device is connected on the VP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

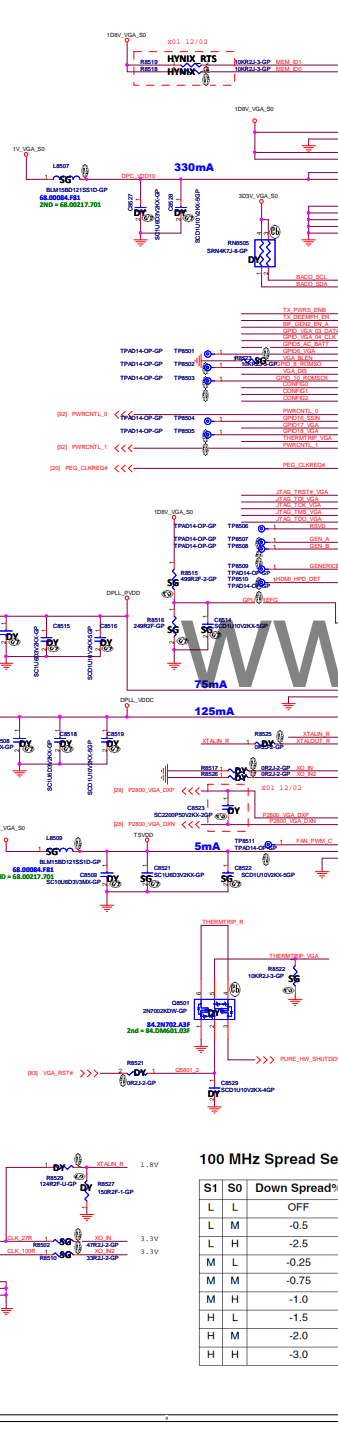
Straps Pin



MEMORY ID Table

DVPPDATA[3:0]	Description
0011	GD8R5 1.250GHz Rynlx-H5Q2H24MFR-T2C 128M*16
0001	GD8R5 1.250GHz Rynlx-H5Q2H24MFR-T2C 128M*16
0000	GD8R5 1.250GHz SAM02NG-R4G20325FD-PC04 128M*16

DVPPDATA[0:3] Default: Pull down



100 MHz Spread Selection Table

S1	S0	Down Spread%
L	L	OFF
L	M	-0.5
L	H	-2.5
M	L	-0.25
M	M	-0.75
M	H	-1.0
H	L	-1.5
H	M	-2.0
H	H	-3.0

100 MHz Spread Selection Table

S1	S0	Down Spread%
L	L	OFF
L	M	-0.5
L	H	-2.5
M	L	-0.25
M	M	-0.75
M	H	-1.0
H	L	-1.5
H	M	-2.0
H	H	-3.0

100 MHz Spread Selection Table

S1	S0	Down Spread%
L	L	OFF
L	M	-0.5
L	H	-2.5
M	L	-0.25
M	M	-0.75
M	H	-1.0
H	L	-1.5
H	M	-2.0
H	H	-3.0

100 MHz Spread Selection Table

S1	S0	Down Spread%
L	L	OFF
L	M	-0.5
L	H	-2.5
M	L	-0.25
M	M	-0.75
M	H	-1.0
H	L	-1.5
H	M	-2.0
H	H	-3.0

100 MHz Spread Selection Table

S1	S0	Down Spread%
L	L	OFF
L	M	-0.5
L	H	-2.5
M	L	-0.25
M	M	-0.75
M	H	-1.0
H	L	-1.5
H	M	-2.0
H	H	-3.0

100 MHz Spread Selection Table

S1	S0	Down Spread%
L	L	OFF
L	M	-0.5
L	H	-2.5
M	L	-0.25
M	M	-0.75
M	H	-1.0
H	L	-1.5
H	M	-2.0
H	H	-3.0

100 MHz Spread Selection Table

S1	S0	Down Spread%
L	L	OFF
L	M	-0.5
L	H	-2.5
M	L	-0.25
M	M	-0.75
M	H	-1.0
H	L	-1.5
H	M	-2.0
H	H	-3.0

100 MHz Spread Selection Table

S1	S0	Down Spread%
L	L	OFF
L	M	-0.5
L	H	-2.5
M	L	-0.25
M	M	-0.75
M	H	-1.0
H	L	-1.5
H	M	-2.0
H	H	-3.0

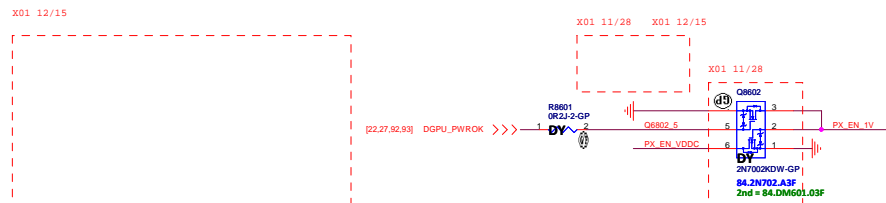
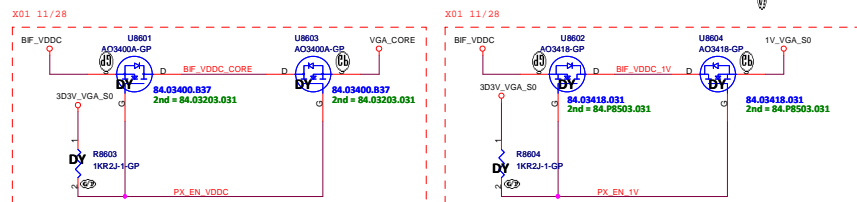
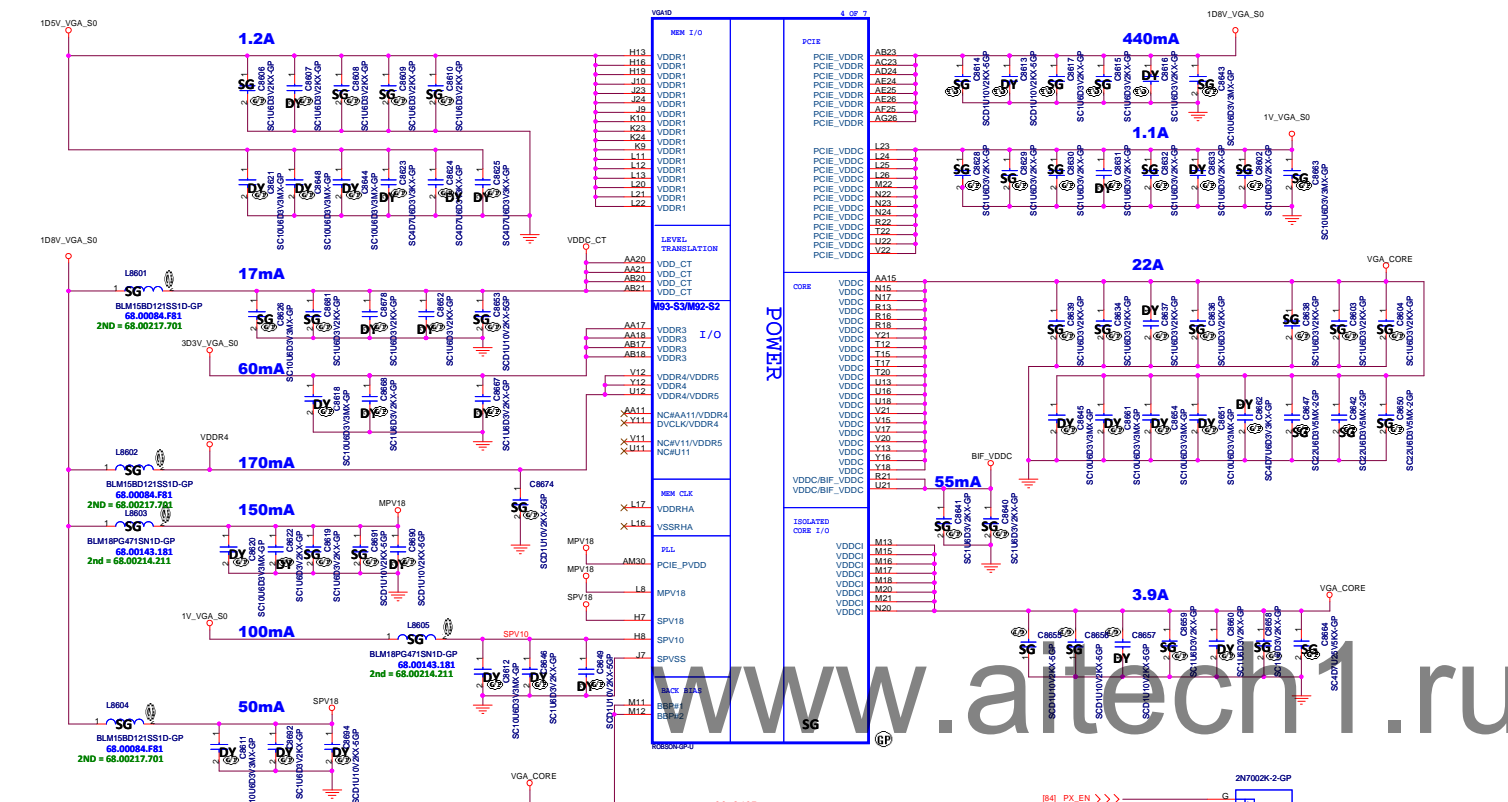
100 MHz Spread Selection Table

S1	S0	Down Spread%
L	L	OFF
L	M	-0.5
L	H	-2.5
M	L	-0.25
M	M	-0.75
M	H	-1.0
H	L	-1.5
H	M	-2.0
H	H	-3.0

100 MHz Spread Selection Table

S1	S0	Down Spread%
L	L	OFF
L	M	-0.5
L	H	-2.5
M	L	-0.25
M	M	-0.75
M	H	-1.0
H	L	-1.5
H	M	-2.0
H	H	-3.0

SSID = VIDEO



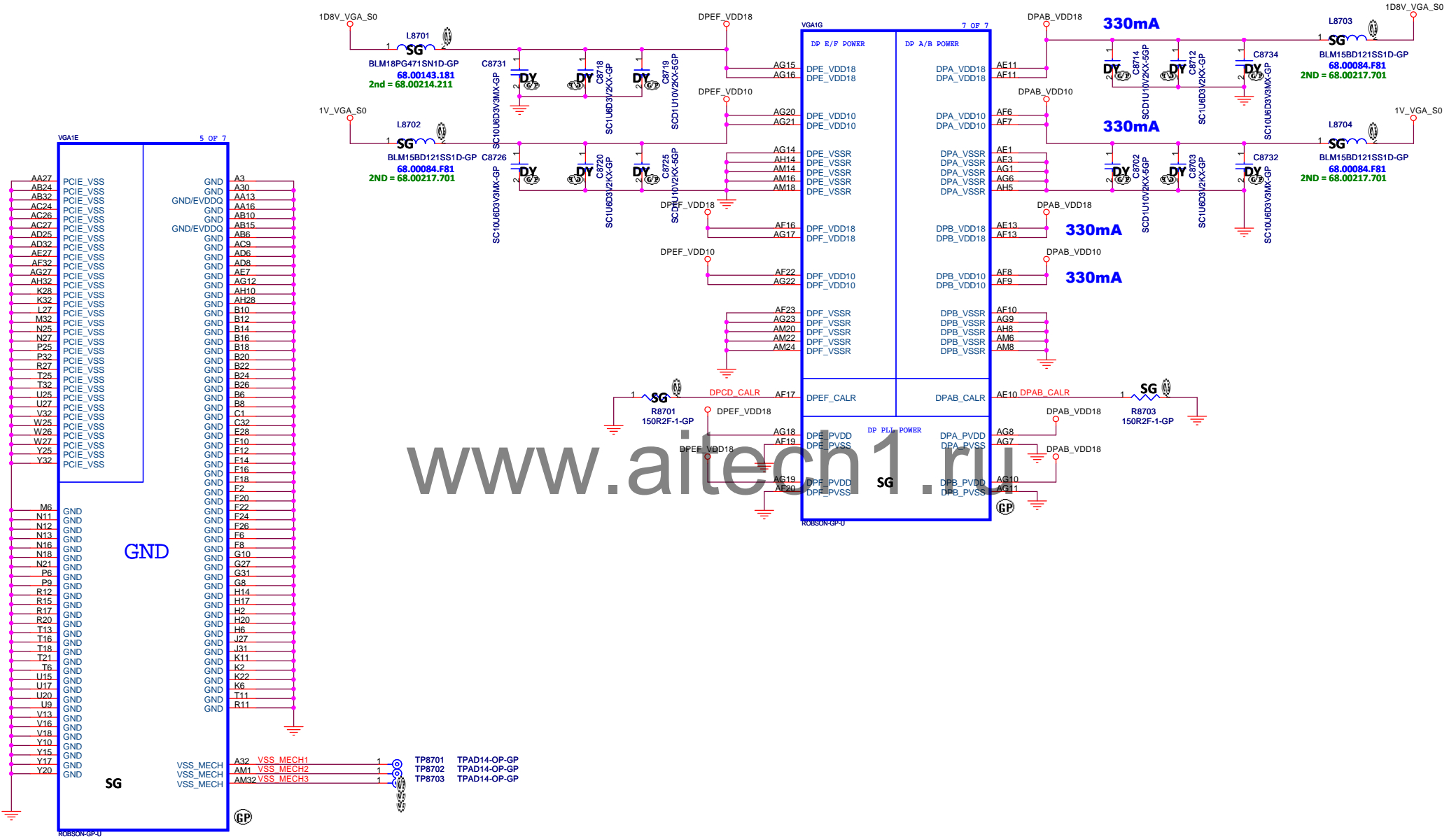
PX4.0				
Mode	PX_EN	PX_EN_1V	PX_EN_VDDC	BIF_VDDC
DIS	Low	Low	High	VGA_CORE
BACO	High	High	Low	1V_VGA_S0

POP	Q8601, Q8602, R8601, U8601, U8602, U8603 U8604, R8603, R8604, R8408
DY	R8612

FX5.0	
POP	R8612
DY	Q8601, Q8602, R8601, U8601, U8602, U8603 U8604, R8603, R8604, R8605, R8408

SSID = VIDEO

For Video output port power rail.



DMB40



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GPU_DPPWR/GND(5/5)Size
A3

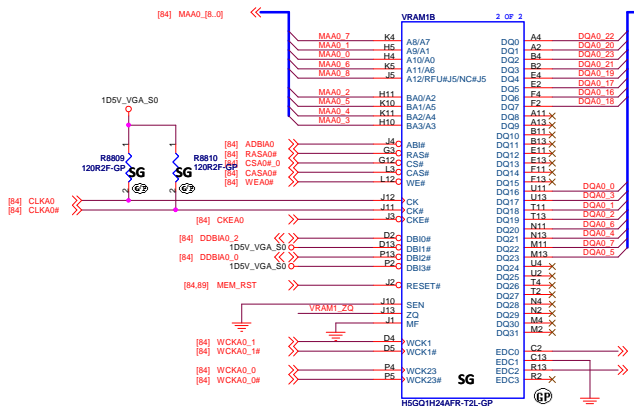
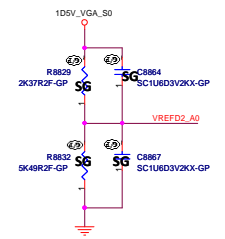
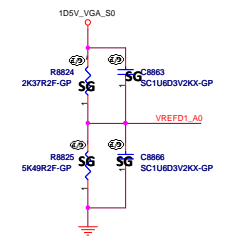
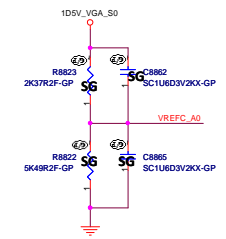
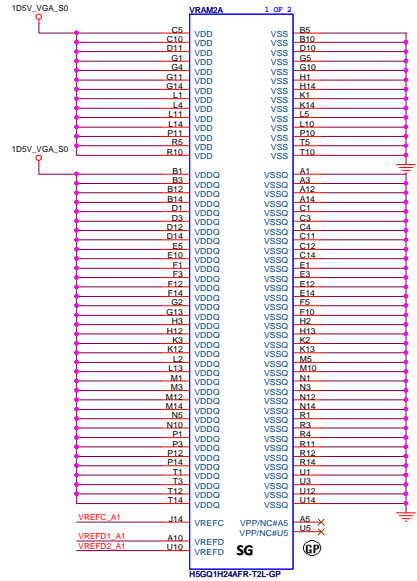
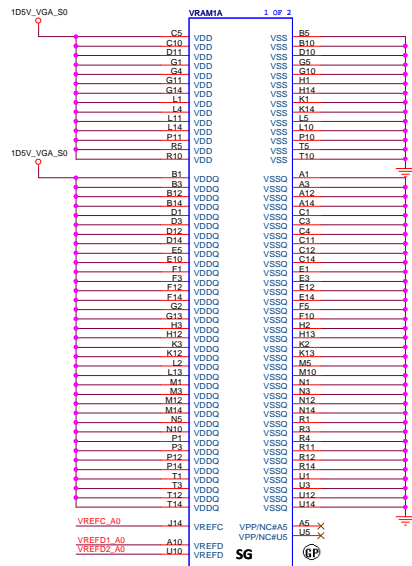
Document Number	
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BMW Z4 DISRev
A00

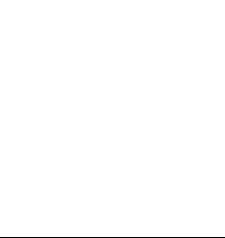
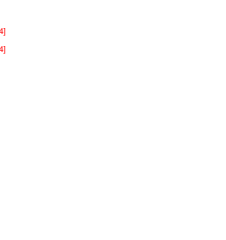
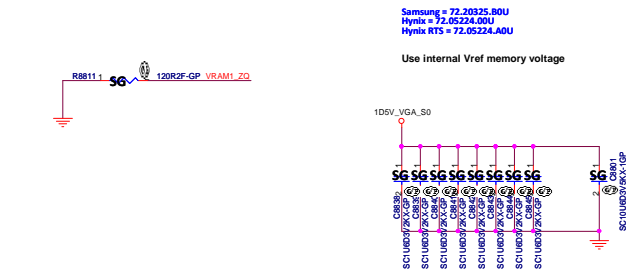
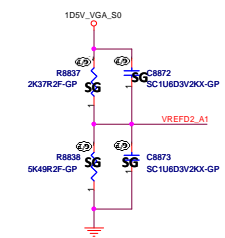
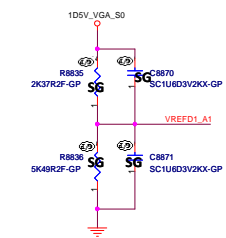
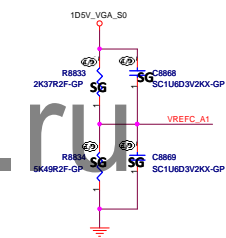
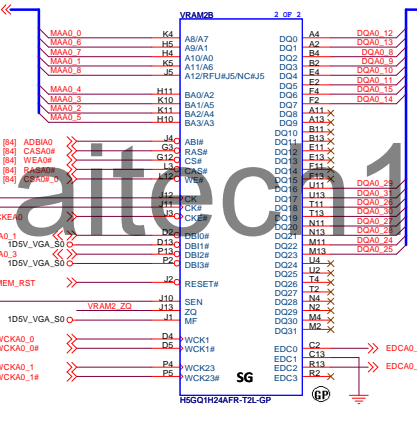
Date: Friday, March 30, 2012

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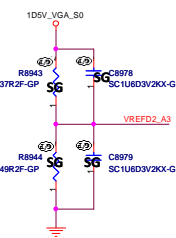
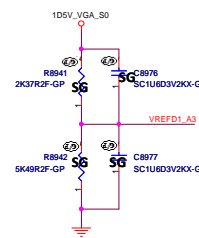
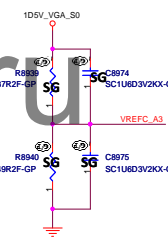
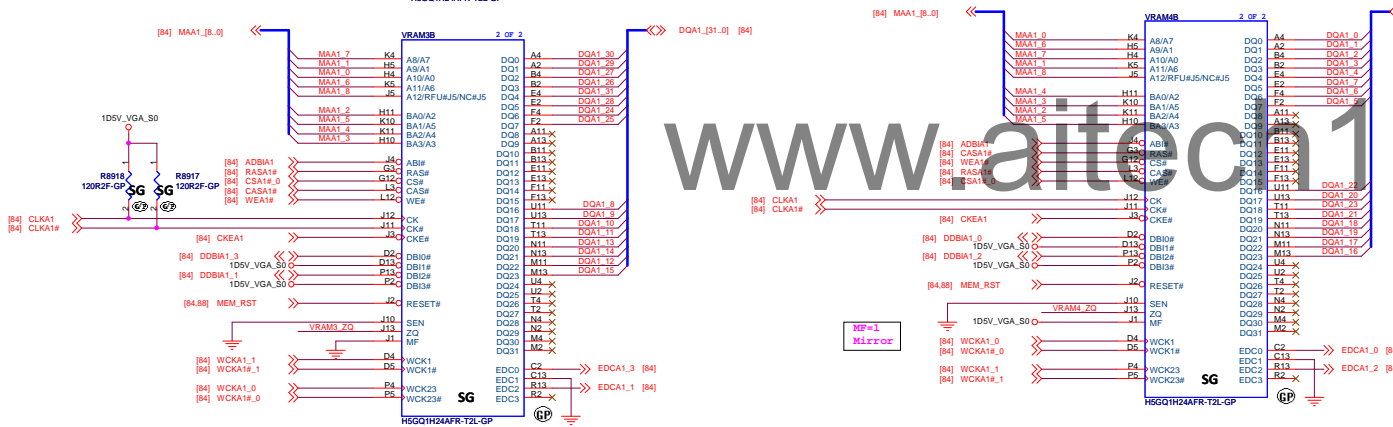
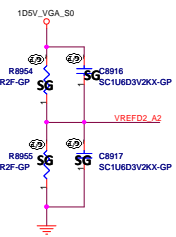
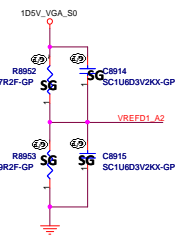
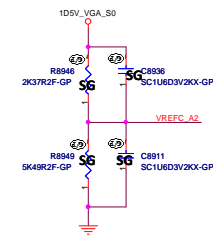
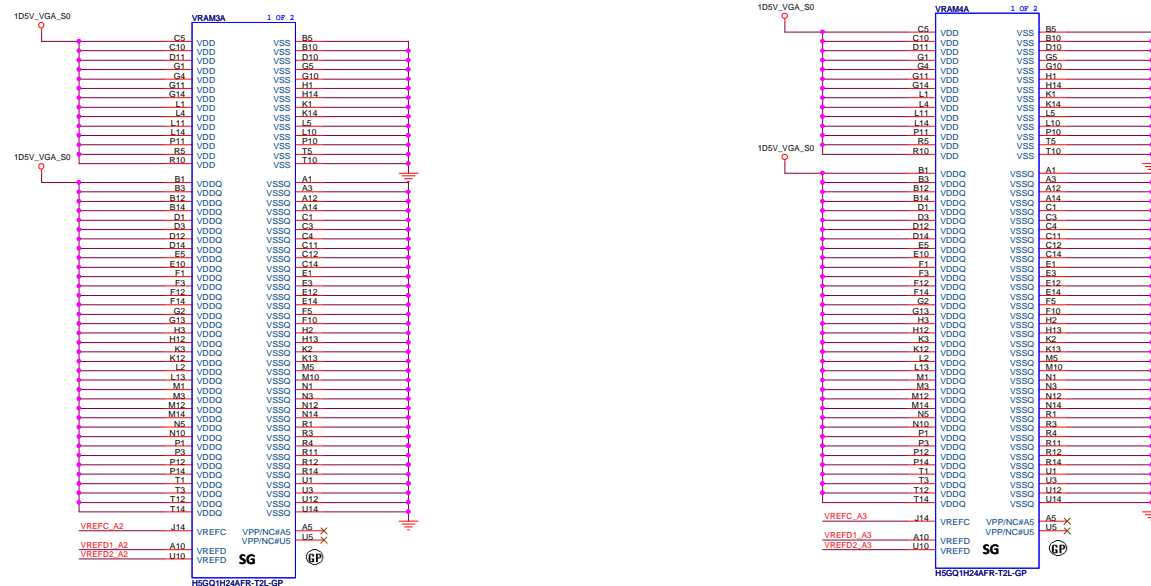
SSID = VIDEO



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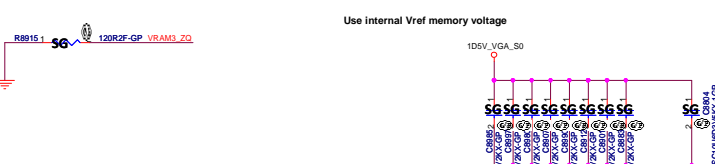


SSID = VIDEO



Samsung = 72.20325.00U
Hynix = 72.05224.00U

Use internal Vref memory voltage



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Title			
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Size A3	Document Number BMW Z4 DIS		Rev A00
Date: Friday, March 30, 2012	Sheet	90	of 105

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Title

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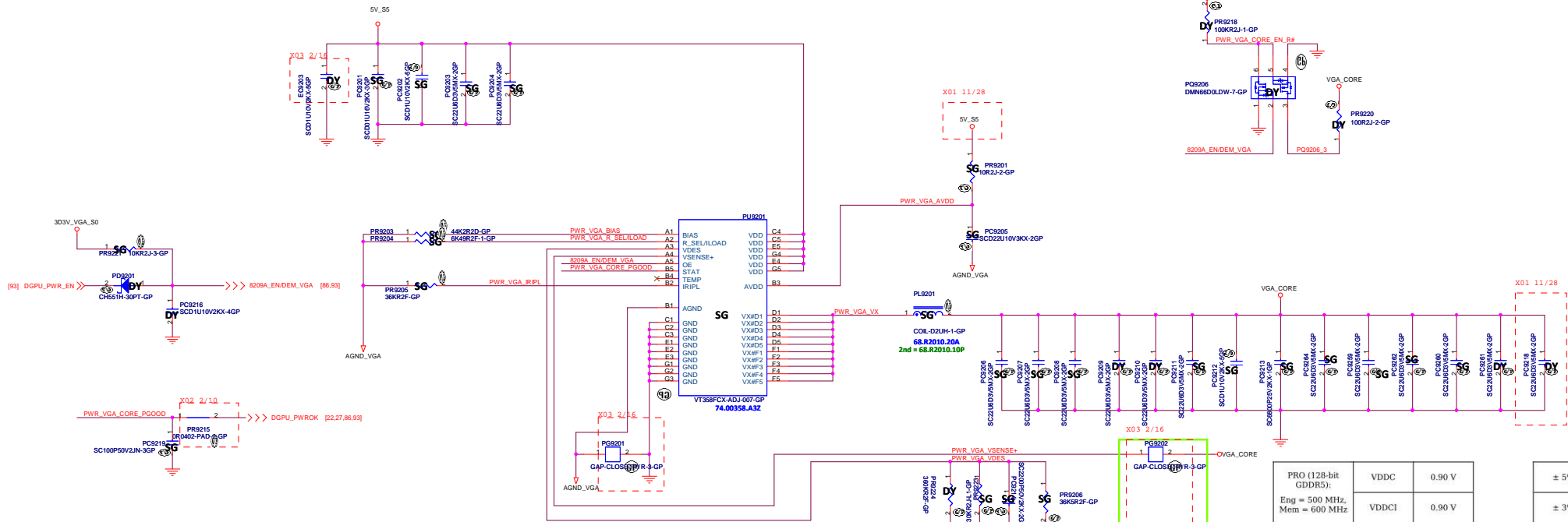
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BMW Z4 DIS

Rev
A00

Date: Friday, March 30, 2012

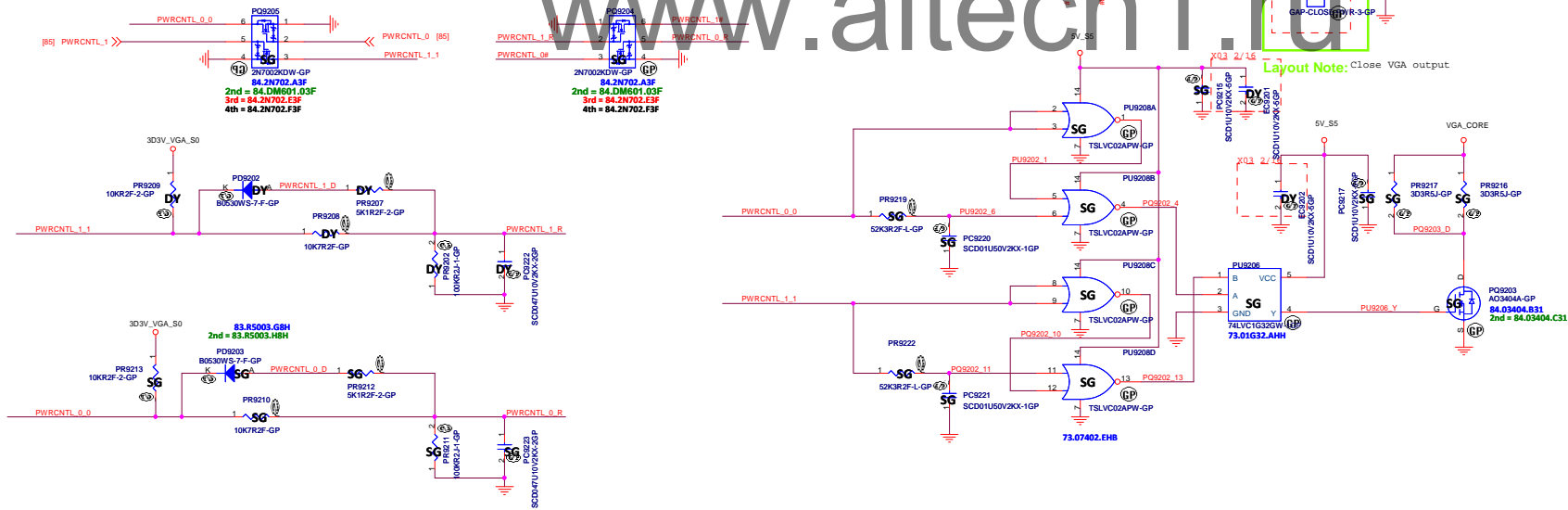
Sheet 91 of 105

```
SSID = PWR.Plane.Regulator_vga_core
```



PRO (128-bit GDDR5): Eng = 500 MHz, Mem = 600 MHz	VDDC	0.90 V	± 5%	16.0 A (RMS) 22.0 A (Peak)
	VDDCI	0.90 V	± 3%	3.3 A (RMS) 3.9 A (Peak)

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VID0 GPIO15	Voltage
1	1V
0	0.9V

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Document Number
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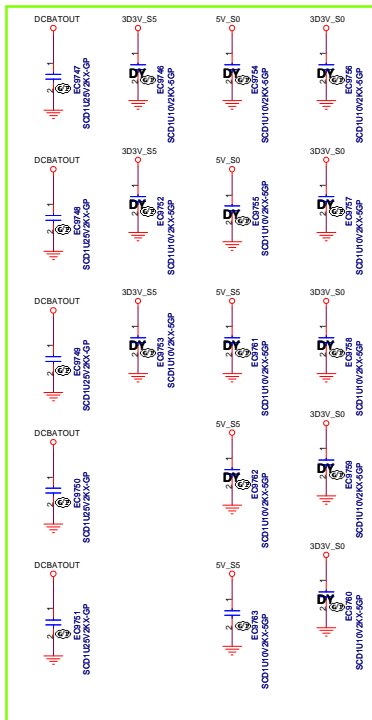
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Rev
A00

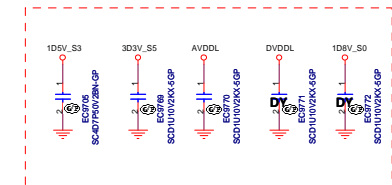
Sheet 96 of 105

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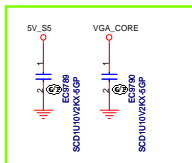
RF



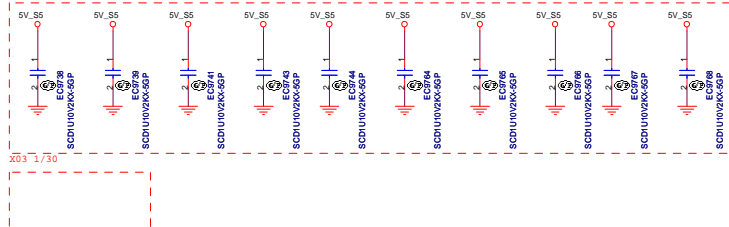
X01 12/15 For RF



X01 12/15 For RF

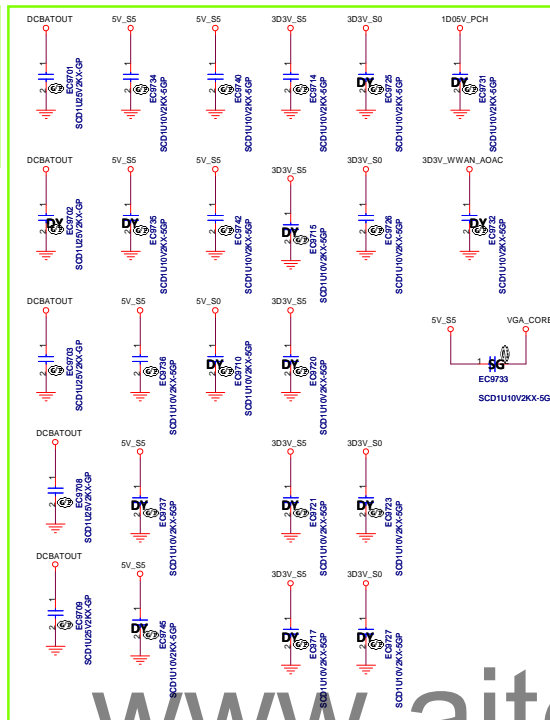


X01 12/09 For EMI X01 12/30

 $\bar{x}03\bar{1}/30$

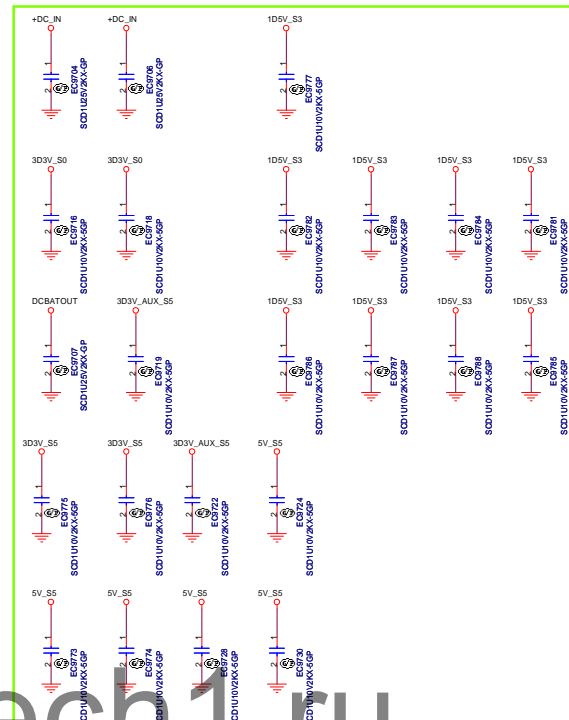
EM

X03 2/13 A00 3/27 A00 3/29

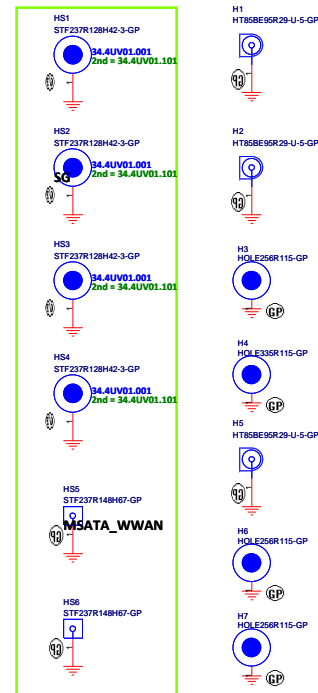


EN

x03 2/16 x03 2/21



On the TOP side

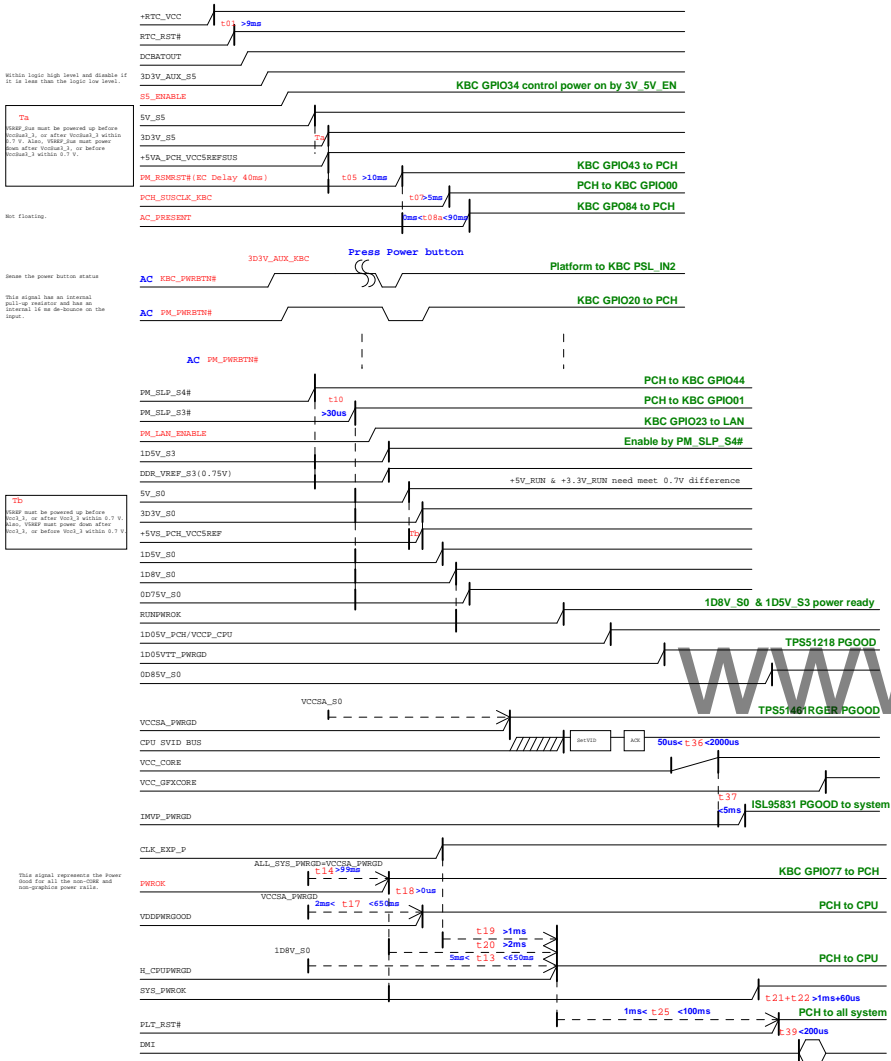


x01 12/

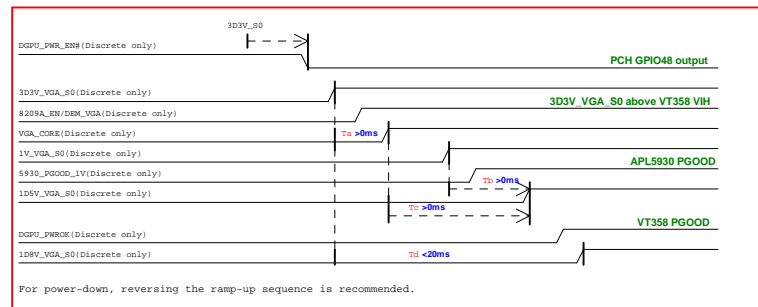
Huron River Platform Power Sequence

(AC mode)

red word: KBC GPIO

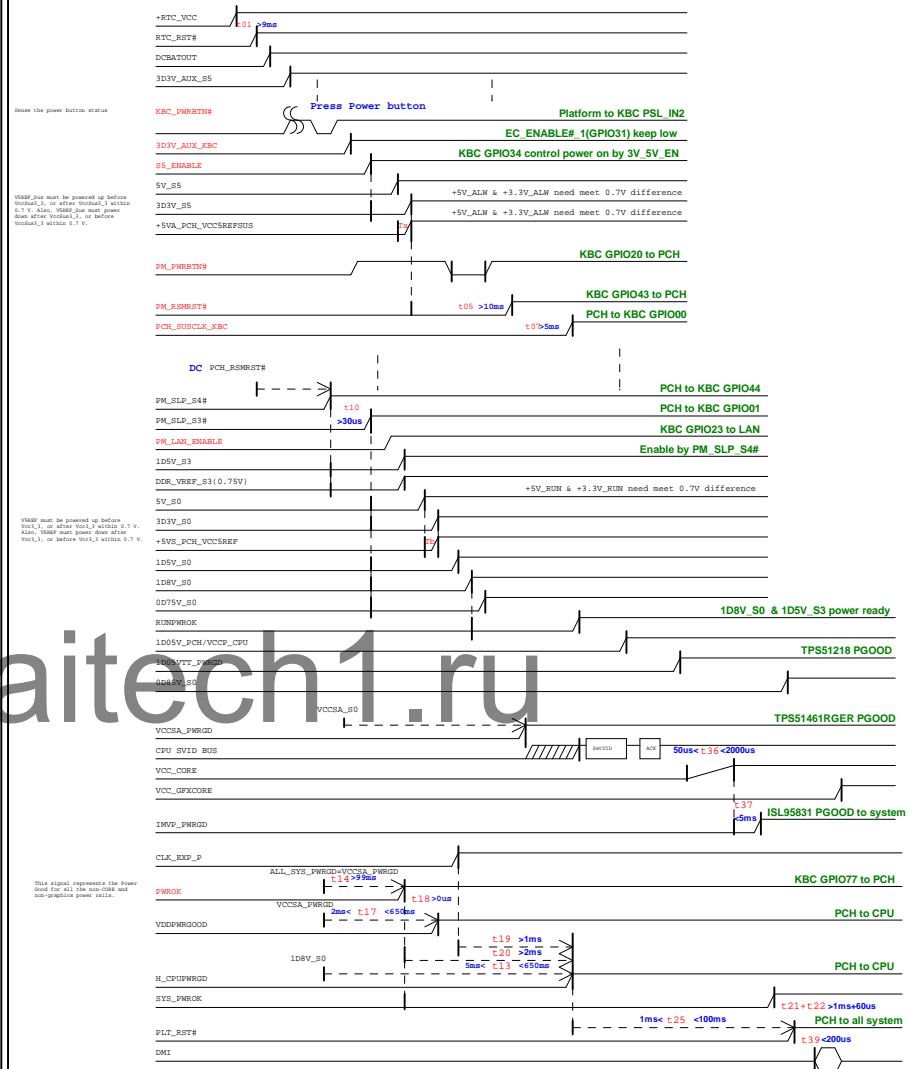


Thames PRO Power-Up/Down Sequence

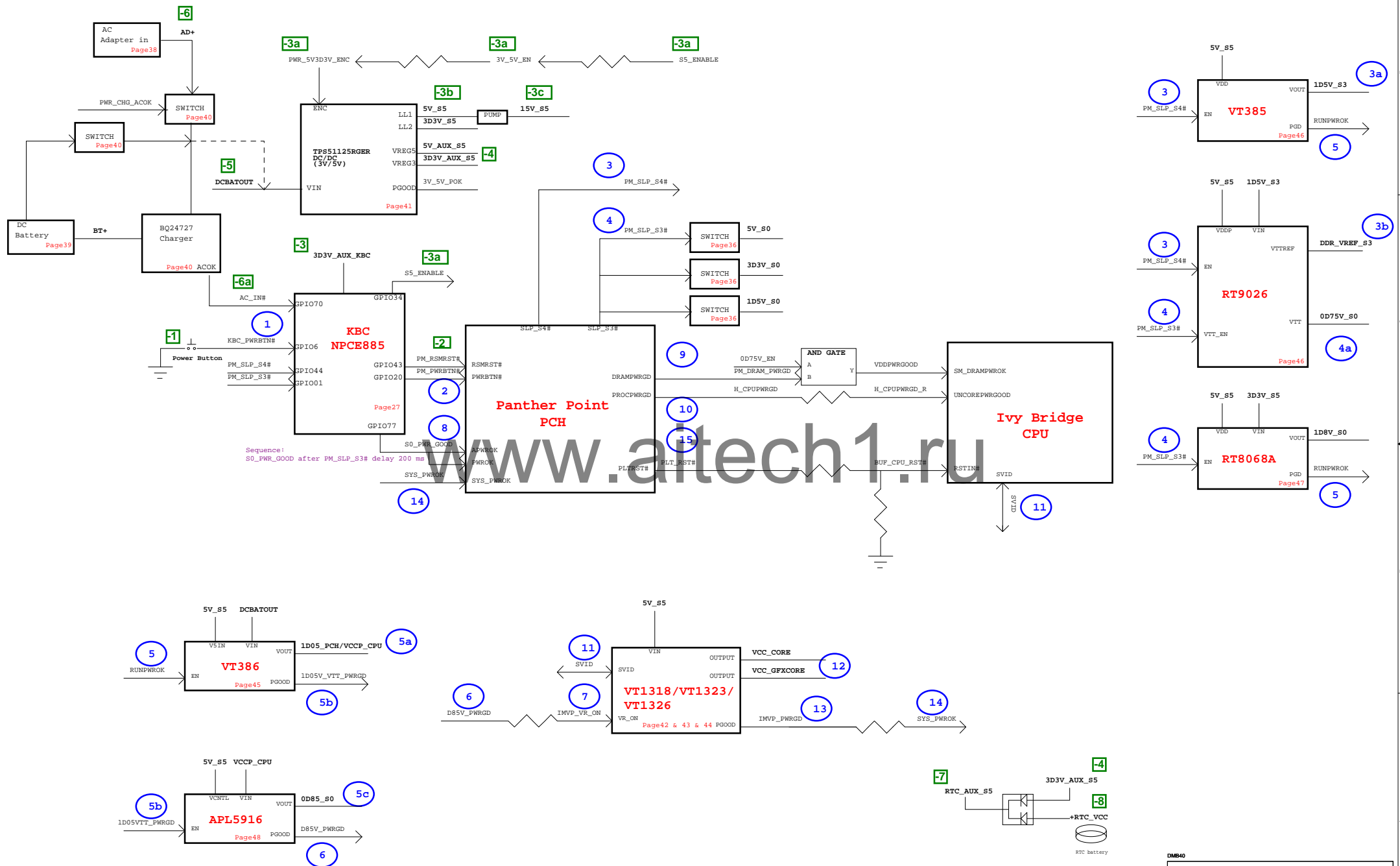


(DC mode)

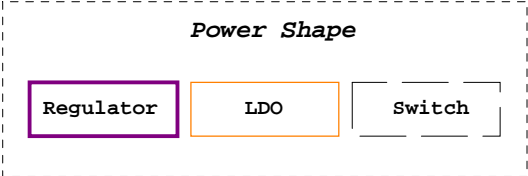
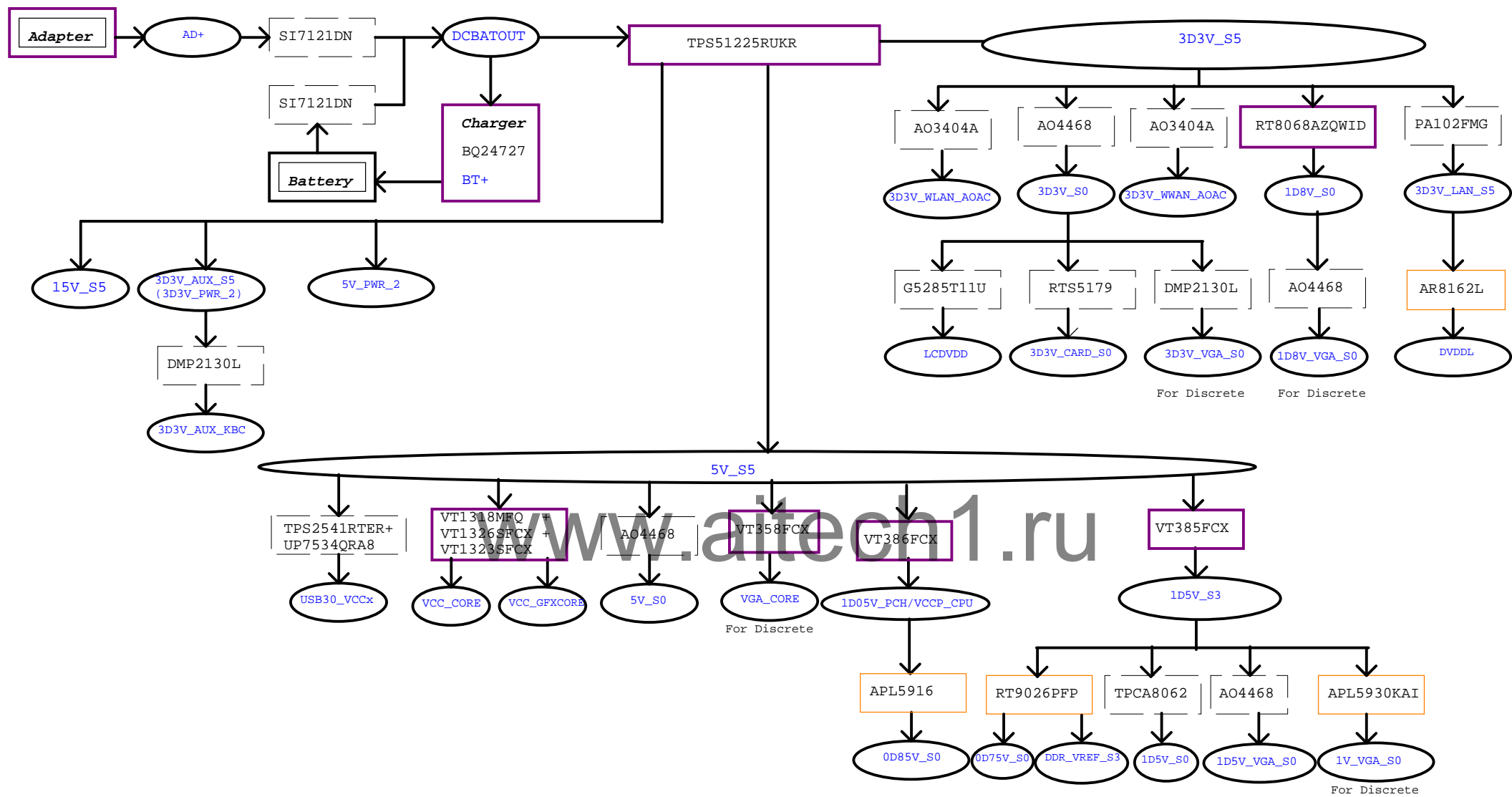
red word: KBC GPIO



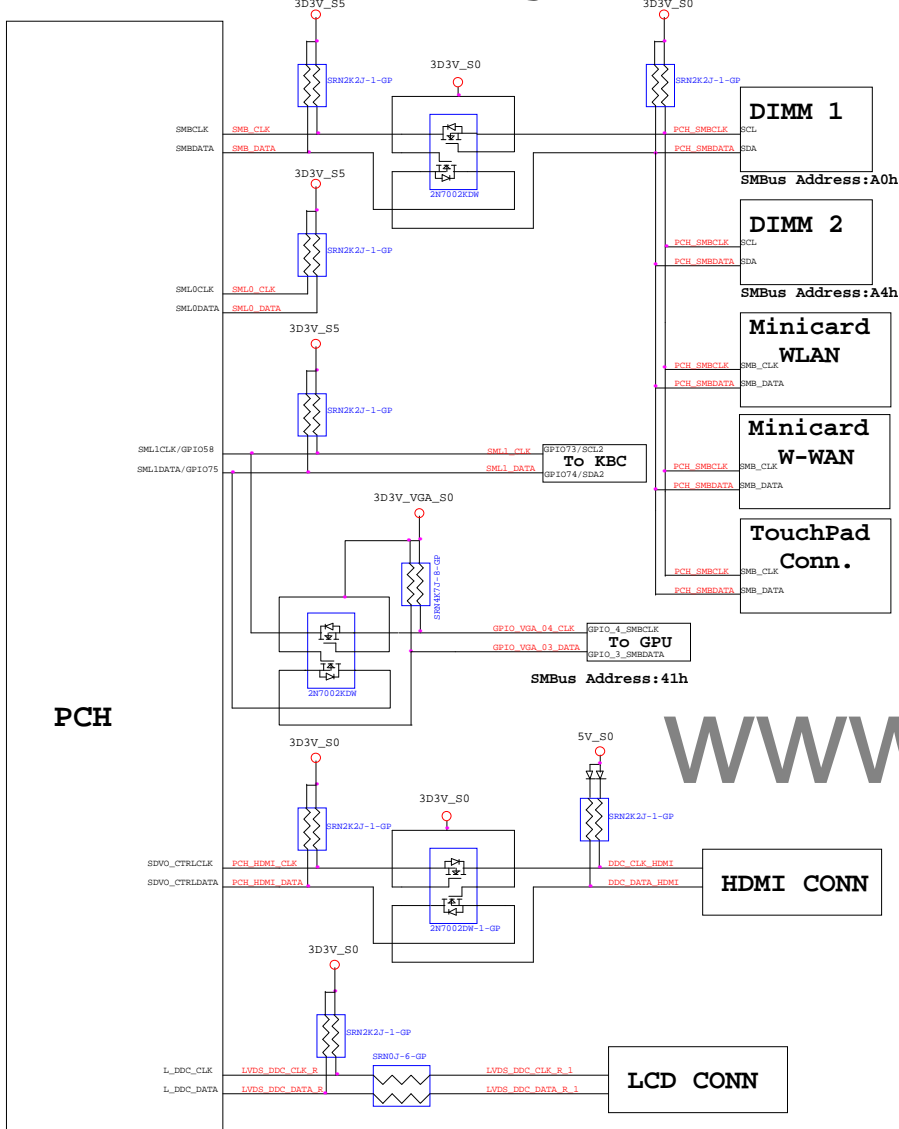
WISTRON CHIEF RIVER POWER UP SEQUENCE DIAGRAM



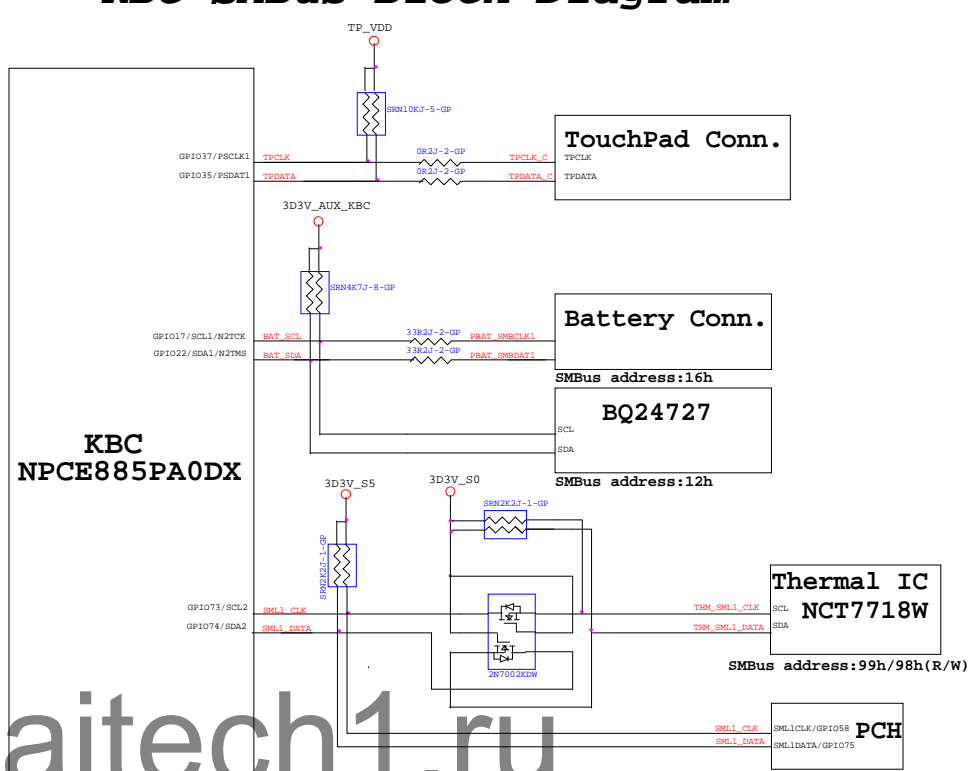
Power Up Sequence: -8 ~ 15



PCH SMBus Block Diagram

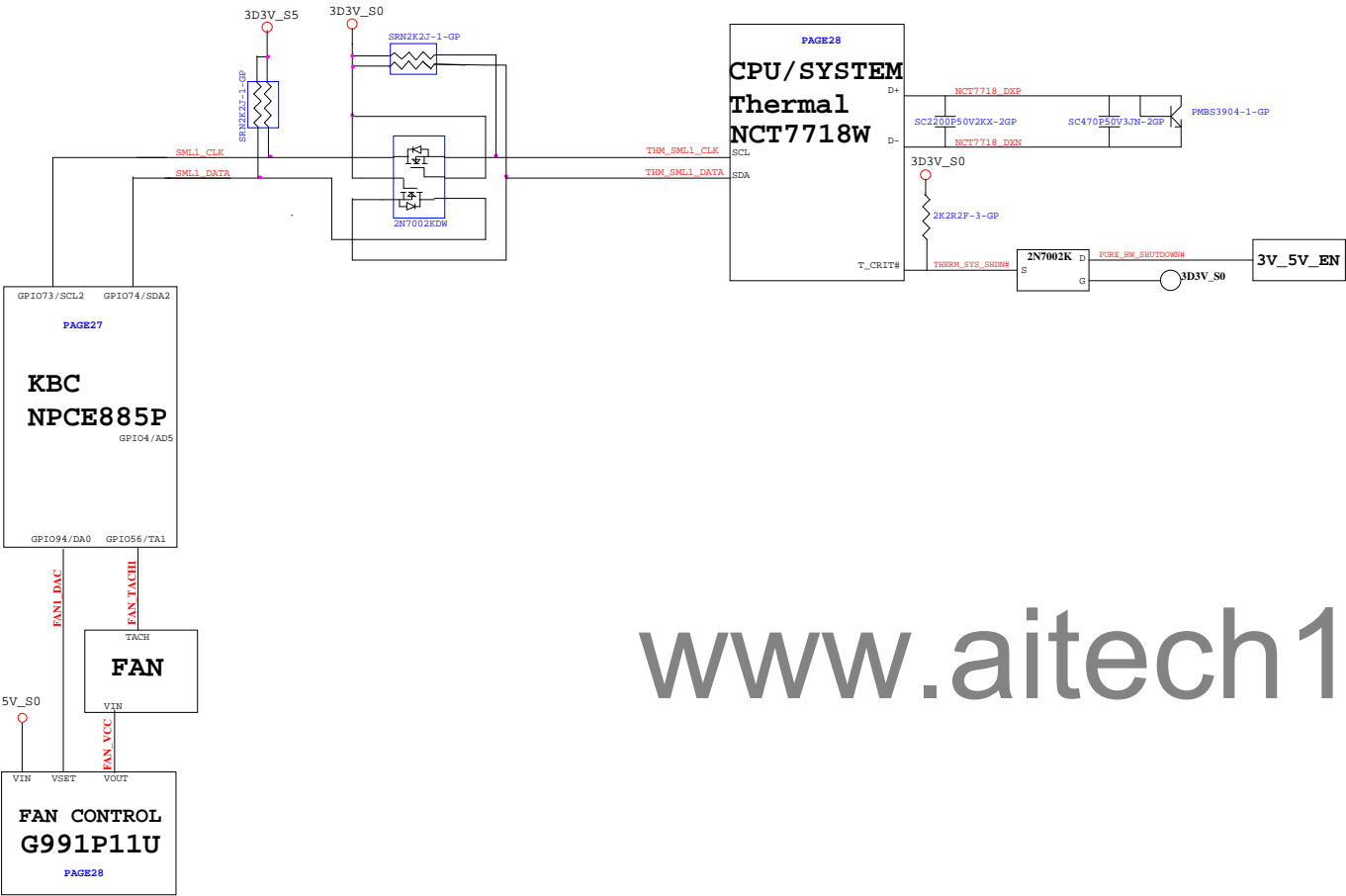


KBC SMBus Block Diagram

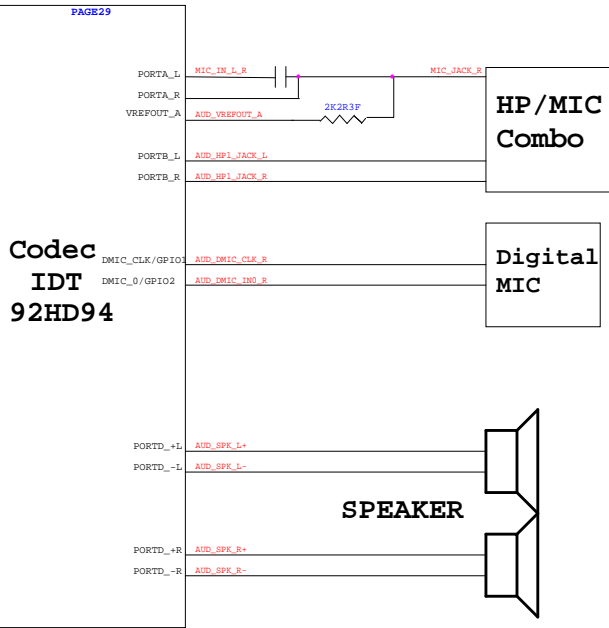


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Thermal Block Diagram



Audio Block Diagram




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DATE	PAGE	Change Item	Owner	Version
2011 11/28	92	Change VT358 AVDD power rail to 5V_S5 to avoid leakage	Power	X01
2011 11/28	92	Re-name Cap PC4663 to PC9218.	EE	X01
2011 11/28	85	Change U8506 power rail and select pin to 3D3V_VGA_S0 to avoid leakage	EE	X01
2011 11/28	93	Change PU9303 to 74.05930.03D by design	EE	X01
2011 11/28	93	POP PD9301, PD9302, PD9303, PD9304, PC9328, change PR9327 to 20K, PR9330 to 10K, PC9326 to 0.1u, PR9312 to 100K, PR9312 re-connect to DGPU_PWR_EN, PD9302 re-connect to DGPU_PWROK for GPU power sequence	EE	X01
2011 11/28	37	Change R3714 to 10K to fix step-like waveform	EE	X01
2011 11/28	84	DY R8408 cause GPU support PX5.0	EE	X01
2011 11/28	86	DY R8605, Q8602, R8603, R8604, U8601, U8602, U8603, U8604, cause GPU support PX5.0	EE	X01
2011 12/02	27	Reserved DGPU_PWROK signal to inform KBC	EE	X01
2011 12/02	62	POP R6208, DY R6201 for USB charging function.	EE	X01
2011 12/02	85	Change VRAM type setting.	EE	X01
2011 12/02	41	Change PT4101, PT4103, PT4104 to 77.52271.09L for design change	EE	X01
2011 12/02	27	Add R2737 for avoiding KBC power drop.	EE	X01
2011 12/02	37	Change R3719 to Q402 type	EE	X01
2011 12/02	69	Change TPAD1 conn by ME	ME	X01
2011 12/02	82	Change LEDBD1 conn by ME	ME	X01
2011 12/02	56	Change HDD1 conn by ME	ME	X01
2011 12/02	68	Change PWSW1 conn by ME	ME	X01
2011 12/02	27	Change RSTSW1 conn by ME	ME	X01
2011 12/02	39	Add BATSW1 and R3901 for avoiding MB crack on assembling.	ME	X01
2011 12/02	60	Change RTC1 conn by ME	ME	X01
2011 12/02	39	DY D3901, D3902, D3903 cause the battery is internal type.	EE	X01
2011 12/02	51	Re-name D5001 and F5001 to D5101 and F5101, and DY F5101 and add R5109 due to no current leakage problem	EE	X01
2011 12/02	14	Change DM1 conn by ME	ME	X01
2011 12/02	27	Change R2724 to 20K for X01 version	EE	X01
2011 12/02	85	DY C8523, cause VGA temp detect by SMBUS.	EE	X01
2011 12/02	28	DY U2803, C2817, C2818 cause VGA temp detect by SMBUS.	EE	X01
2011 12/02	38	Del PR3812.	EE	X01
2011 12/02	49	Change LCD1 conn by ME	ME	X01
2011 12/02	60	POP U6001 and del ROMSK1 for X01 version	EE	X01
2011 12/02	65	Change R6507 to J type	EE	X01
2011 12/02	39	Change BATT1 conn by ME	ME	X01
2011 12/02	82	Change IOBD1 conn by ME	ME	X01
2011 12/02	68	Add WLAN/WWAN LED power control circuit	EE	X01

DATE	PAGE	Change Item	Owner	Version
2011 12/09	27	Change AOAC_PCIE_WAKE# pull high to 3D3V_WLAN_AOAC and PCIE_WAKE# to 3D3V_LAN_S5	EE	X01
2011 12/09	66	Change WWAN power to 3D3V_S0	EE	X01
2011 12/09	8	Change VCC_CORE MLCC by power team request	Power	X01
2011 12/09	9	Change AXG_CORE MLCC by power team request	Power	X01
2011 12/09	22	Reserved DGPU_HOLD_RST# & DGPU_PWR_EN# pull high and down	EE	X01
2011 12/09	97	Follow EMI request added Cap.	EMI	X01
2011 12/09	20	Rename PCIE request pin	EE	X01
2011 12/09	65	Add WLAN requirist circuit	EE	X01
2011 12/12	40	design change PU4001 by Power team request	Power	X01
2011 12/12	41	design change PU4106 by Power team request	Power	X01
2011 12/12	41	Change PU4102 to colay symbol by Power team request	Power	X01
2011 12/12	45	Change PU4501to VT386 by Power team request	Power	X01
2011 12/12	46	Change PR4609 and PR4612 by Power team request	Power	X01
2011 12/12	48	Change PU4801 by Power team request	Power	X01
2011 12/12	43	Reserved PT4301 by Power team request	Power	X01
2011 12/12	84	Change R8412 to 4.7k.	EE	X01
2011 12/12	27	Change U2701 to new P/N	EE	X01
2011 12/13	82	Add ER8201, ER8202, ER8203, ER8204 by EMI request.	EMI	X01
2011 12/13	18	Reserved USB_PN13, USB_PP13 test point.	EE	X01
2011 12/13	62	Del USB3.0 Redriver circuit.	EE	X01
2011 12/13	27	Change R2735 and R2737 to 20K for fix AUX power overshoot.	EE	X01
2011 12/13	41	Change PC4127 to 4.7uF for fix AUX power overshoot.	EE	X01
2011 12/13	82	Add ER8205, EC8206 by EMI request.	EMI	X01
2011 12/13	46	Add EL4601, EL4602 by EMI request.	EMI	X01
2011 12/13	43	Add EG4301,EG4302EG4303,EG4304,EG4305,EG4306,EG4307 by EMI request.	EMI	X01
2011 12/13	44	Add EG4401,EG4402,EG4403,EG4404,EG4405,EG4406,EG4407 by EMI request.	EMI	X01
2011 12/13	15	Change DM2 conn by ME request	ME	X01
2011 12/15	97	Add EC9736, EC9726, EC9750 EC9708, EC9709, EC9770, EC9705, EC9769 by RF request.	RF	X01
2011 12/15	56	Add EC5601 by RF request.	RF	X01
2011 12/15	46	Add EC4638 by RF request.	RF	X01
2011 12/15	31	Add EC3122 by RF request.	RF	X01

<Core Design>



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DATE	PAGE	Change Item	Owner	Version
2011 12/15	14	Change DM1 P/N to 62.10017.S81	EE	X01
2011 12/15	15	Change DM2 P/N to 62.10017.T01	EE	X01
2011 12/15	62	Del R6201 change by USB detect function	EE	X01
2011 12/15	65	DY R6507, U6501 for design change	EE	X01
2011 12/15	68	Add R6809, DY C6802, R6803, D6802, WLAN LED power control by AOAC_WLAN_EN#.	EE	X01
2011 12/15	8	Change C825, C830, C831, C832 to 0805 type.	EE	X01
2011 12/15	9	Change C906, C907, C908, C909, C910 to 0805 type.	EE	X01
2011 12/15	93	Del 1D8V_VGA_S0 power good circuit.	EE	X01
2011 12/15	83	Del VGA_RST# circuit.	EE	X01
2011 12/15	86	Del 1D5V_VGA_S0 power good circuit.	EE	X01
2011 12/15	31	Reserved EC3101 by RF request.	RF	X01
2011 12/15	97	Reserved EC9771, EC9772 by RF request.	RF	X01
2011 12/16	86	Change C8642, C8650, C8647 to 22u 0805 size.	EE	X01
2011 12/16	62	Pop TR6204, DY R6279, R6280.	EMI	X01
2011 12/16	49	Pop TR4902, DY R4903, R4906.	EMI	X01
2011 12/16	8	Change C847 to 22u 0805 size.	EE	X01
2011 12/16	68	Pop C6802, for soft start.	EE	X01
2011 12/19	38	Change PC3806 to 0805 type	Power	X01
2011 12/19	43	Del PT4301 cause no layout area.	Power	X01
2011 12/20	44	Change PWR_GFX to PWR_CPU	Power	X01
2011 12/20	18	Change touch panel USB signal to port 4.	EE	X01
2011 12/20	82	Reserved TPAN1, and swap IOBD1's main and 2nd source.	EE	X01
2011 12/20	49	Swap LCD1's main and 2nd source.	EE	X01
2011 12/20	14	Change R1401, R1402 to short pad	EE	X01
2011 12/20	15	Change R1502 to short pad	EE	X01
2011 12/20	39	Change R3902, R3903, R3904 to 100 ohm to avoid break KBC when battery in.	EE	X01
2011 12/20	27	Del RN2703, add R2714, R2715.	EE	X01
2011 12/21	48	POP PR4814, change PR4811 to 365ohm, PR4813 to 100Kohm	Power	X01
2011 12/21	21	Add R2115 and del R6001 for SPI louting setting	EE	X01
2011 12/21	8	DY C807, C843, C824.	Power	X01
2011 12/21	42	Change PR4236 to 374ohm, PR4249 to 7.68Kohm.	Power	X01
2011 12/21	43	Change PU4301 IC to lastly version.	Power	X01
2011 12/21	44	Change PU4401 IC to lastly version.	Power	X01
2011 12/21	40	Design change PU4002 by power request	Power	X01
2011 12/21	27	Add R2716 to modify PSL circuit.	EE	X01
2011 12/23	82	Swap USB1, USB10 signal to TR8202 TR8201 for layout	EE	X01

DATE	PAGE	Change Item	Owner	Version
2011 12/23	62	Swap USB0 signal to TR6204 for layout	EE	X01
2011 12/23	97	Del H8.	ME	X01
2011 12/27	51	Pop D5101, DY R5109.	EE	X01
2011 12/30	93	Change PD9301, PD9302, PD9303, PD9304's 2nd source to 83.R5003.H8H	EE	X01
2011 12/30	31	Change U3101 to 71.08162.A03 due to vendor update new version.	EE	X01
2011 12/30	97	Pop EC9738, EC9739, EC9741, EC9743, EC9744, EC9764, EC9765, EC9766, EC9767, EC9768	EMI	X01
2011 12/30	36, 93	Change U3601 U3602 PU9305 PU9306 2nd to 84.04178.037	Power	X01
2011 12/30	49	Change TR4902 to 69.10103.041	EMI	X01
2012 01/09	15, 24	DY C1507 and C2403 by PI testing result.	EE	X01
2012 01/09	48	Change VCCSA to LDO type.	Power	X02
2012 01/09	51	Change HDMI SMBUS pull up power to 5V_HDMI_S0_R	EE	X03
2012 01/30	48	Reserved PC4818 PC4819 to prevent VCCSA power IC VID setting(PWM solution)	EE	X03
2012 01/30	68	Add D6803 to fix DW1703 BT LED behavior. and change WLAN LED power rail to 5V_S0.	EE	X03
2012 01/30	97, 38	Take off EC9704, del PS_ID_R.	EE	X03
2012 01/30	82	Move IO BD conn signal for coaxial cable	EE	X03
2012 01/30	66	DY R6615.	EE	X03
2012 01/30	40, 38	Change PR4004 to 3K and PR3816 to 3.3K for hiccup mode adaptor.	EE	X03
2012 01/30	62	Change U6201 to lastly version.	EE	X03
2012 01/30	31	Change L3101 to prevent the shortage problem.	EE	X03
2012 02/06	82	Change TPAN1 P/N by ME request and modify conn pin define.	EE	X03
2012 02/06	31	Reserved C3110 for Lan IC.	EE	X03
2012 02/06	5, 8, 9, 14, 15, 19, 23, 24, 27, 28, 36, 37, 38, 49, 51, 62, 65, 66, 83, 85	Change R504, R812, R909, R1404, R1405, R1505, R1503, R1921, R1916, R1924, R1929, R1925, R2304, R2301, R2307, R2306, R2308, R2403, R2404, R2412, R2402, R2702, R2765, R2794, R2778, R2792, R2733, R2767, R2768, R2720, R2764, R2723, R2727, R2807, R3614, R3710, PR3819, R4912, R4913, R5125, R5101,R5102, R5149, R5103, R5108, R5107, R5106, R5105, R6202, R6203, R6204, R6205, R6505, R6502, R6616, R8322, R8504, R8506, R8507, to short pad	EE	X03
2012 02/10	41, 42, 45, 46, 47, 95	Change PR4127, PR4130, PR4133, PR4116, PR4251, PR4250, PR4212, PR4207, PR4228, PR4523, PR4522, PR4510, PR4511, PR4626, PR4621, PR4622, PR4623, PR4611, PR4602, PR4702 ,PR9215 to short pad	Power	X03
2012 02/13	51	Change HDMI output power design	EE	X03
2012 02/13	41, 42, 18 19, 28, 93	Change PR9311, PR9320, PR4116, PR4219, PR4223, PR4252, PR4254, PR4261, R1823, R1927 R2813 to short pad	Power	X03
2012 02/13	97	Add EC9704, EC9706, EC9716, EC9718, EC9722, EC9724, EC9728, EC9730, EC9775, EC9776, EC9773, EC9774,EC9701, EC9751, EL4901 by EMI required	EMI	X03



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